Instruction Manual

Tektronix

TMS 540
PowerPC 60X Microprocessor Support

070-9829-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 540 PowerPC 60X microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 540 PowerPC 60X support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with PPC60X. This is the name of the microprocessor in field selections and file names you must use to operate the PowerPC 60X support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 136-channel or a 192-channel module.
- PPC60X refers to all supported variations of the PowerPC 60X microprocessor unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 540 microprocessor support package
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 540 microprocessor support package disassembles data from systems that are based on Motorola MPC601, MPC603, and MPC604 microprocessors, and IBM PPC601, PPC603 and PPC604 microprocessors. The Motorola MPC604 and IBM PPC604 microprocessors are only supported through the software setup and disassembler.

The support runs on a compatible Tektronix logic analyzer equipped with a 136-channel module or a 192-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 540 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 540 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
Motorola MPC601	304-pin QFP
Motorola MPC603	240-pin QFP
Motorola MPC604*	304-pin QFP
IBM PPC601	304-pin QFP
IBM PPC603	240-pin QFP
IBM PPC604*	304-pin QFP

*** Contact Tektronix for availability of the MPC604 or PPC604 microprocessor support.**

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following documents:

- The *PowerPC System Architecture Manual*, Mindshare, Inc.,1995
- The *PowerPC Microprocessor Family: The Programming Environments Manual*, Motorola, Inc., 1993
- The *PowerPC 601 RISC Microprocessor User's Manual*, Motorola, Inc., 1993
- The MPC601 data sheet, Motorola, Inc., 1993
- The *PowerPC 603 RISC Microprocessor User's Manual*, IBM Microelectronics, and Motorola, Inc., 1993
- The *PowerPC 603 RISC Microprocessor Hardware Specification*, IBM Microelectronics, and Motorola, Inc., 1993
- The *PowerPC 604 RISC Microprocessor User's Manual*, IBM Microelectronics, and Motorola, Inc., 1993

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the PowerPC 60X support, the Tektronix logic analyzer must be equipped with either a 136-channel module, or a 192-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your PowerPC 60X-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other PowerPC 60X support requirements and restrictions.

System Clock Rate. The TMS 540 support can acquire data from the PowerPC 60X microprocessor at speeds of up to 66 MHz[1].

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

PPC601 SYSCLK Signal. When connecting to a PPC601 microprocessor system under test, the HI_C3:3, HI_CK3, and LO_CK3 podlets must connect to a 1X clock. When using the TMS 540 product, the application assumes that the BCLK_EN* signal is a 1X clock. If it is not, you must remove the jumper on J300 on the probe adapter and connect a 1X clock to pin 2 of J300.

For the relationship between the clock and signals to be correct, you need to compare the 1X clock to the TS* and TA* signals with a 200 MHz oscilloscope. There should be 6 ns setup time between the assertion of TS* and TA* (going low) and the rising clock edge of the 1X clock. To improve the clock trace, you can add a small ferrite bead to the wire connecting the 1X clock to pin 2 of J300.

MPC604 and PPC604 Microprocessor Support. The Motorola MPC604 and IBM PPC604 microprocessors are only supported through the application setup and disassembler. You can, however, use a commercial test clip and the PPC60X probe adapter to connect to the signals in you SUT. Refer to the connection procedure beginning on page 1–11.

Address Pipelining. If address pipelining sustains for many sequences (approximately 1 K), there might be performance degradation when scrolling data by entering a sequence number in the Cursor field.

If address pipelining sustains for additional sequences (1 K or greater), there might be erroneous address and data association. You can use the Mark Cycles function to correct the interpretation of erroneous address and data association.

Configuring the Probe Adapter

The probe adapter does not require any configuration.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 136-channel module. The probes will look different if you are using a 192-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

MPC601, PPC601, MPC603, and PPC603 Converter Clips

This procedure requires contact lubricant and thermal joint compound. To connect the logic analyzer to a SUT using a QFP probe adapter and PGA-to-QFP converter clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the acquisition probes, or the module. To prevent static damage, handle all the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the probe adapter might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal surface.
4. Use a magnifying glass to examine the pins of the microprocessor soldered into the SUT. Check for the following characteristics:
   a. The pins are cleanly soldered to the board without excess solder or deformity.
   b. The bends of the pins are uniform (consistent and even).
5. Apply contact lubricant to the pins of the converter clip to improve the connection to the microprocessor.

6. Check that the heat sink moves easily, and yet stays in position when not being moved.

   If the heat sink is very difficult to move or does not stay in position, you need to adjust the friction of the O-ring in the PGA-to-QFP converter clip. To adjust the friction, refer to Figure 1–1 and follow these steps:

   a. If you have difficulty moving the heat sink, loosen each of the four O-ring screws a little until the heat sink is moveable, and yet will stay in position.

   b. If the heat sink does not stay in position, tighten each of the four O-ring screws a little until the heat sink is moveable, and yet will stay in position.

CAUTION. *Do not loosen or tighten the four screws closest to the corners of the PGA-to-QFP converter clip. These are set by the manufacturer.*

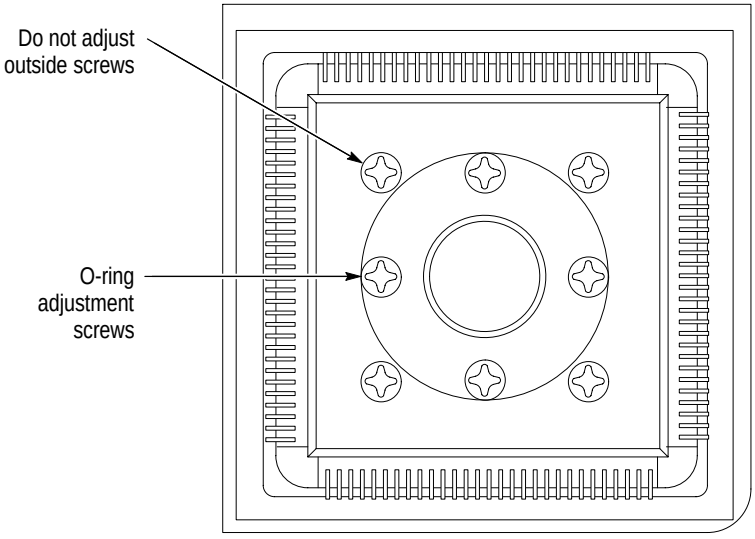


Figure 1–1: Adjusting the friction of the O-ring in the converter clip

7. Pull up the heat sink on the converter clip to allow vertical clearance for the microprocessor.

8. Apply a small amount of thermal joint compound to the end of the heat sink that faces the microprocessor (the end that will contact the microprocessor).

CAUTION. *Failure to correctly place the PGA-to-QFP converter clip onto the microprocessor might permanently damage the microprocessor and converter clip once power is applied.*

9. Line up the pin E1 indicator on the converter clip with the pin 1 indicator on the microprocessor.

10. Place the converter clip onto the microprocessor as shown in Figure 1–2. Center the clip on the microprocessor and press the clip down while slightly rocking the clip.

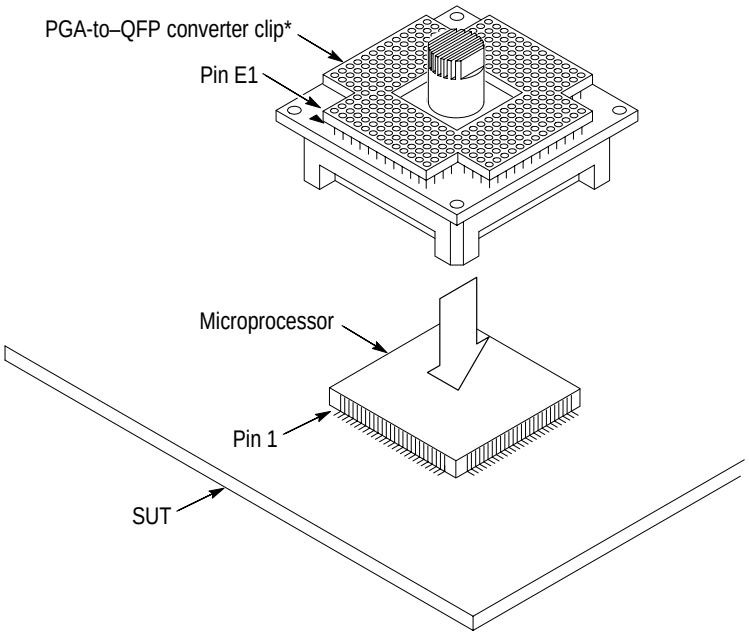


Figure 1–2: Placing the PGA-to-QFP converter clip onto the microprocessor

11. Measure the resistance between Vcc and ground to verify that they are not shorted together. If you detect a short, determine the source and repair the problem before applying power (described at the end of this chapter).

12. If there are tie-down holes in your SUT that match the tie-down holes on the converter clip, you can use screws to secure the clip (and probe adapter) to the SUT.

Figure 1–3 shows the placement of the tie-down holes on the MPC601 or PPC601 clips. Figure 1–4 shows the placement of the tie-down holes on the MPC603 or PPC603 clips.

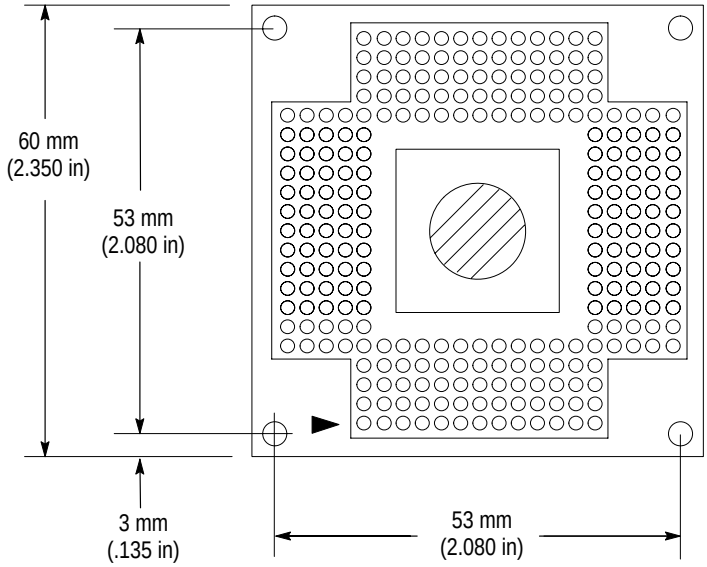


Figure 1–3: Tie-down hole placement on the MPC601 or PPC601 converter clips

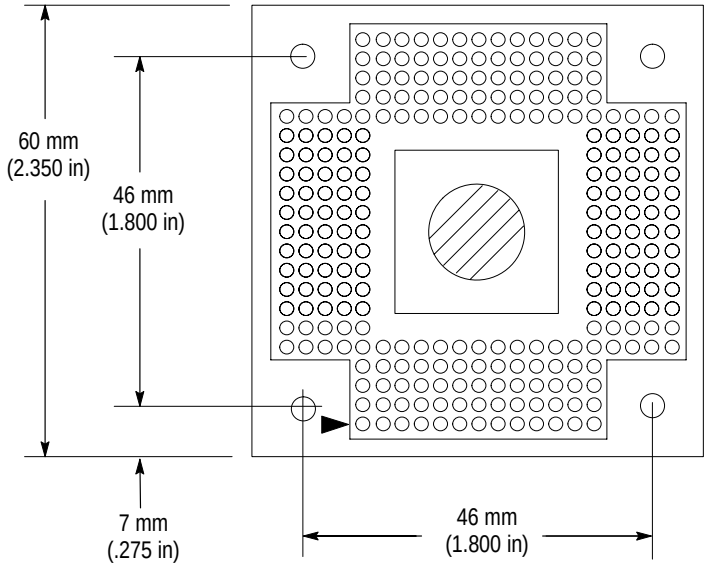


Figure 1–4: Tie-down hole placement on the MPC603 or PPC603 converter clips

13. Gently press down and turn the heat sink in the converter clip until it just makes contact with the microprocessor.

14. If you cannot secure the clip through tie-down holes and screws, you can use a nonconductive retention device around the clip and SUT circuit board to make sure the clip is secure. Figure 1–5 shows an example of this method.

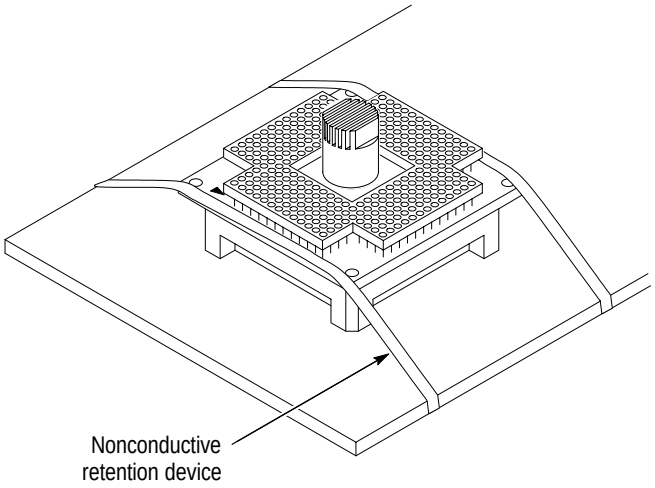


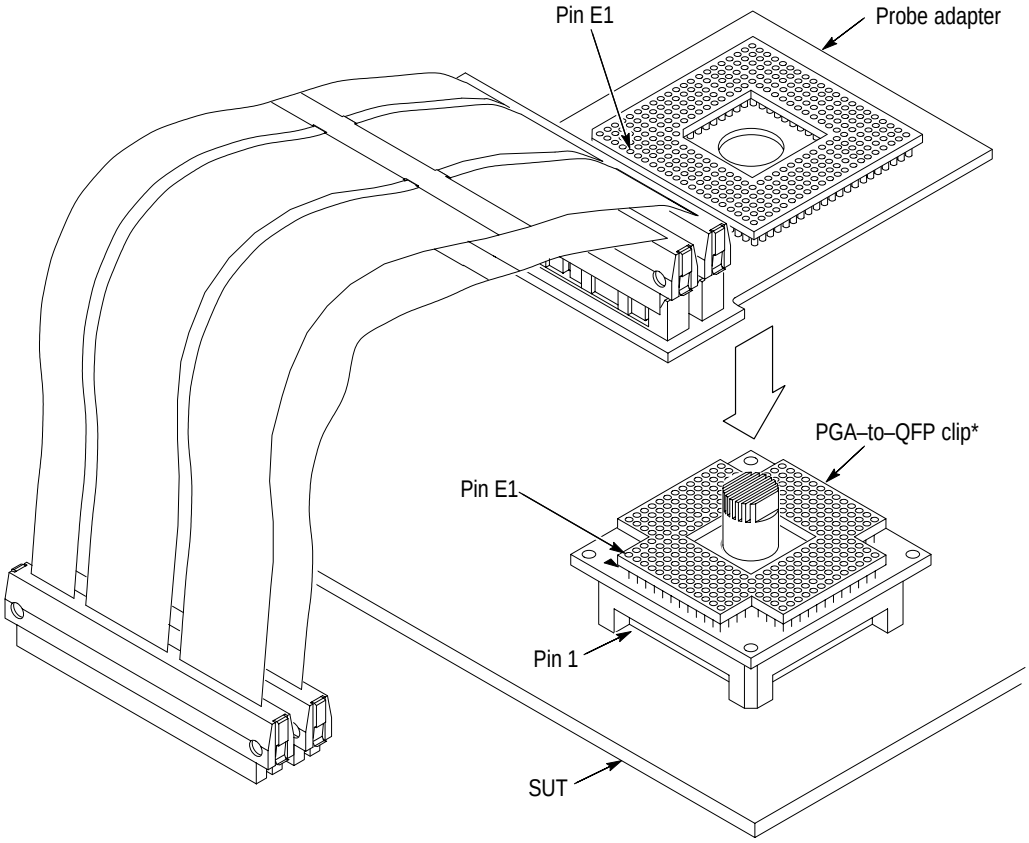
Figure 1–5: Using an alternate method to secure the PGA-to-QFP converter clip

CAUTION. *Failure to correctly place the probe adapter onto the PGA-to-QFP converter clip might permanently damage the microprocessor, probe adapter, and clip once power is applied.*

15. Remove the black foam from the underside of the probe adapter.

16. Line up the pin E1 indicator on the probe adapter with the pin E1 indicator on the PGA-to-QFP clip.

17. Place the probe adapter onto the PGA-to-QFP clip as shown in Figure 1–6.



* Earlier versions of some clips might not have a heat sink.

Figure 1–6: Placing the probe adapter onto the PGA-to-QFP converter clip

18. Connect the clock and channel probes to the high-density probe as shown in Figure 1–7. For the 192-channel module, match the channel groups and numbers on the probe labels to the corresponding HI_ and LO_pins on the high-density probe. Match the ground pins on the probes to the corresponding pins on the probe adapter.

For the 136-channel module, match the channel groups and numbers on the probe labels to the corresponding LO_ pins on the high-density probe. There are some exceptions; they are shown in Table 1–2.

Table 1–2: High-density probe exceptions for the 136-channel module

Section	Connect to high-density probe pins
E3, E2, E1, E0	HI_A3, HI_A2, HI_A1, HI_A0
C1, C0	HI_C3, HI_C2

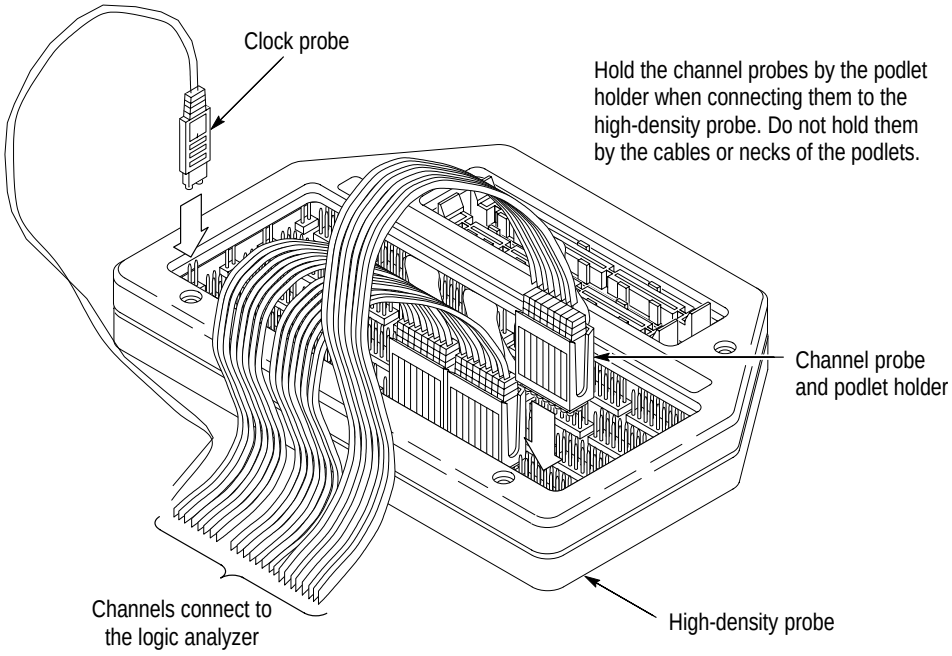


Figure 1–7: Connecting probes to a high-density probe

19. Align pin 1 on the LO cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the LO connector on the high-density probe. Connect the cable to the connector as shown in Figure 1–8.

NOTE*. The LO cable is 12 inches long; the HI cable is 13 inches long.*

20. Align pin 1 on the HI cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the HI connector on the high-density probe. Connect the cable to the connector as shown in Figure 1–8.

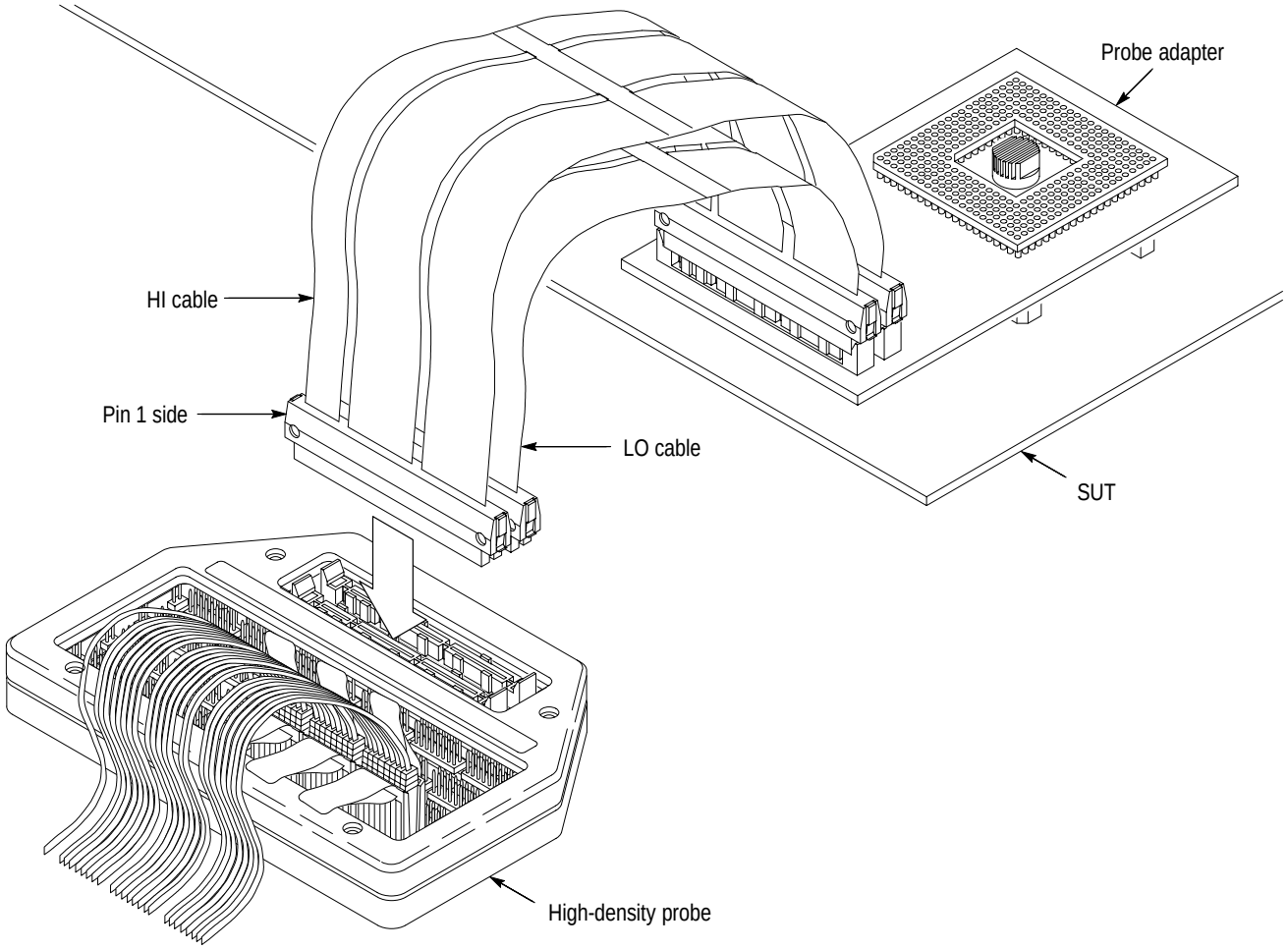


Figure 1–8: Connecting cables to a high-density probe

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to PowerPC 60X signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. For the 136-channel module, use Tables 1–3 and 1–6 to connect the channel and clock probes to PowerPC 60X signal pins on a test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins in your SUT or on your test clip.

Table 1–3: 136-channel: PowerPC 60X connections for channel probes

Section:channel	PowerPC 60X signal	Section:channel	PowerPC 60X signal
A3:7	A0	D3:7	DL0
A3:6	A1	D3:6	DL1
A3:5	A2	D3:5	DL2
A3:4	A3	D3:4	DL3
A3:3	A4	D3:3	DL4
A3:2	A5	D3:2	DL5
A3:1	A6	D3:1	DL6
A3:0	A7	D3:0	DL7
A2:7	A8	D2:7	DL8
A2:6	A9	D2:6	DL9
A2:5	A10	D2:5	DL10
A2:4	A11	D2:4	DL11
A2:3	A12	D2:3	DL12
A2:2	A13	D2:2	DL13
A2:1	A14	D2:1	DL14
A2:0	A15	D2:0	DL15

Table 1–3: 136-channel: PowerPC 60X connections for channel probes (cont.)

Section:channel	PowerPC 60X signal	Section:channel	PowerPC 60X signal
A1:7	A16	D1:7	DL16
A1:6	A17	D1:6	DL17
A1:5	A18	D1:5	DL18
A1:4	A19	D1:4	DL19
A1:3	A20	D1:3	DL20
A1:2	A21	D1:2	DL21
A1:1	A22	D1:1	DL22
A1:0	A23	D1:0	DL23
A0:7	A24	D0:7	DL24
A0:6	A25	D0:6	DL25
A0:5	A26	D0:5	DL26
A0:4	A27	D0:4	DL27
A0:3	A28	D0:3	DL28
A0:2	A29	D0:2	DL29
A0:1	A30	D0:1	DL30
A0:0	A31	D0:0	DL31
E3:7	DH0	C3:7	TT3
E3:6	DH1	C3:6	TT2
E3:5	DH2	C3:5	TEA*†
E3:4	DH3	C3:4	BG*
E3:3	DH4	C3:3	TSIZ2
E3:2	DH5	C3:2	TBST*
E3:1	DH6	C3:1	TT0
E3:0	DH7	C3:0	XATS_B2* (Delayed XATS*)
E2:7	DH8	C2:7	TSIZ1
E2:6	DH9	C2:6	TSIZ0
E2:5	DH10	C2:5	DBB*
E2:4	DH11	C2:4	ABB*
E2:3	DH12	C2:3	XATS*
E2:2	DH13	C2:2	TS*
E2:1	DH14	C2:1	AACK*
E2:0	DH15	C2:0	ARTRY_ERLY*
E1:7	DH16	C1:7	TC0
E1:6	DH17	C1:6	ARTRY*

Table 1–3: 136-channel: PowerPC 60X connections for channel probes (cont.)

Section:channel	PowerPC 60X signal	Section:channel	PowerPC 60X signal
E1:5	DH18	C1:5	BR_SHD*‡§
E1:4	DH19	C1:4	DBG*
E1:3	DH20	C1:3	SYSCLK‡¶
E1:2	DH21	C1:2	DRTRY*
E1:1	DH22	C1:1	HRESET*‡
E1:0	DH23	C1:0	DRTRY_ERLY*
E0:7	DH24	C0:7	TT1
E0:6	DH25	C0:6	TA*#
E0:5	DH26	C0:5	GBL*
E0:4	DH27	C0:4	DBWO*
E0:3	DH28	C0:3	XATS*=
E0:2	DH29	C0:2	TS*=
E0:1	DH30	C0:1	AACK*=
E0:0	DH31	C0:0	ARTRY_DATA*

† **TEA* is also probed by CK:0.**

‡ **Signal not required for disassembly.**

§ **BR* signal on the 603 microprocessor; SHD* signal on the 601 microprocessor.**

¶ **SYSCLK* is also probed by CK:3.**

\# **TA* is also probed by CK:1.**

5. For the 192-channel module, use Tables 1–4, 1–5, and 1–6 to connect the HI and LO module probes to PowerPC 60X signal pins on a test clip or in the SUT.

For both modules, use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins in your SUT or on your test clip.

Table 1–4 shows the 192-channel HI module probes and the PPC60X signals to which they must connect for disassembly to be correct.

Table 1–4: 192-channel: PowerPC 60X connections for the HI module

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
A3:7	DH0	D3:7	DPE*†
A3:6	DH1	D3:6	DP7†

Table 1–4: 192-channel: PowerPC 60X connections for the HI module (cont.)

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
A3:5	DH2	D3:5	DP6†
A3:4	DH3	D3:4	DP5†
A3:3	DH4	D3:3	DP4†
A3:2	DH5	D3:2	DP3†
A3:1	DH6	D3:1	DP2†
A3:0	DH7	D3:0	DP1†
A2:7	DH8	D2:7	DP0†
A2:6	DH9	D2:6	RSRV*†
A2:5	DH10	D2:5	TC1†
A2:4	DH11	D2:4	WT*†
A2:3	DH12	D2:3	TT4†
A2:2	DH13	D2:2	SRESET*†
A2:1	DH14	D2:1	INT*†
A2:0	DH15	D2:0	APE*†
A1:7	DH16	D1:7	AP3†
A1:6	DH17	D1:6	AP2†
A1:5	DH18	D1:5	AP1†
A1:4	DH19	D1:4	AP0†
A1:3	DH20	D1:3	CI*†
A1:2	DH21	D1:2	SCAN_CTL (601) †
A1:1	DH22	D1:1	SCAN_SIN (601) †
A1:0	DH23	D1:0	SCAN_CLK (601) †
A0:7	DH24	D0:7	SC_DRIVE (601) †
A0:6	DH25	D0:6	CSE1 (601 and 604) †
A0:5	DH26	D0:5	CSE2 (601) †
A0:4	DH27	D0:4	CSE0 (601 and 604) †
A0:3	DH28	D0:3	BSCAN_EN* (601) †
A0:2	DH29	D0:2	PCLK_EN* (601) †
A0:1	DH30	D0:1	RESUME (601) †
A0:0	DH31	D0:0	ESP_EN* (601) †
C3:7	TC0	C1:7	RTC (601) †
C3:6	ARTRY*‡	C1:6	SYS_QUIESC* (601) †

Table 1–4: 192-channel: PowerPC 60X connections for the HI module (cont.)

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
C3:5	BR* (603 and 604), SHD* (601) †	C1:5	CKSTP_IN* (601) †
C3:4	DBG*	C1:4	QUIESC_REQ (601) †
C3:3	SYSCLK†§	C1:3	HP_SNP_REQ* (601) †
C3:2	DRTRY*	C1:2	SCAN_OUT (601) †
C3:1	HRESET*†	C1:1	RUN_NSTOP (601) †
C3:0	DRTRY*	C1:0	CKSTP_OUT* (601) †
C2:7	TT1	C0:7	DBDIS* (603 and 604) †
C2:6	TA*¶	C0:6	TLBISYNC* (603) †
C2:5	GBL*	C0:5	TBEN (603 and 604) †
C2:4	DBWO*	C0:4	QACK* (603) †
C2:3	XATS*#	C0:3	QREQ* (603) †
C2:2	TS*%	C0:2	CSE (603) †
C2:1	AACK*@	C0:1	CLK_OUT (603 and 604) †
C2:0	ARTRY*‡	C0:0	TCK (603 and 604) †

† **Not required for disassembly.**

‡ **ARTRY* is also probed by LO_C2:0.**

§ **SYSCLK is also probed by HI_CLK:3 and LO_CLK:3.**

¶ **TA* is also probed by HI_CLK:1 and LO_CLK:1.**

\# **XATS* is also probed by LO_C3:0 and LO_C2:3.**

% **TS* is also probed by LO_C2:2.**

@ **AACK* is also probed by LO_C2:1.**

Table 1–5 shows the 192-channel LO module probes and the PPC60X signals to which they must connect for disassembly to be correct.

Table 1–5: 192-channel: PowerPC 60X connections for the LO module

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
A3:7	A0	D3:7	DL0
A3:6	A1	D3:6	DL1
A3:5	A2	D3:5	DL2
A3:4	A3	D3:4	DL3

Table 1–5: 192-channel: PowerPC 60X connections for the LO module (cont.)

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
A3:3	A4	D3:3	DL4
A3:2	A5	D3:2	DL5
A3:1	A6	D3:1	DL6
A3:0	A7	D3:0	DL7
A2:7	A8	D2:7	DL8
A2:6	A9	D2:6	DL9
A2:5	A10	D2:5	DL10
A2:4	A11	D2:4	DL11
A2:3	A12	D2:3	DL12
A2:2	A13	D2:2	DL13
A2:1	A14	D2:1	DL14
A2:0	A15	D2:0	DL15
A1:7	A16	D1:7	DL16
A1:6	A17	D1:6	DL17
A1:5	A18	D1:5	DL18
A1:4	A19	D1:4	DL19
A1:3	A20	D1:3	DL20
A1:2	A21	D1:2	DL21
A1:1	A22	D1:1	DL22
A1:0	A23	D1:0	DL23
A0:7	A24	D0:7	DL24
A0:6	A25	D0:6	DL25
A0:5	A26	D0:5	DL26
A0:4	A27	D0:4	DL27
A0:3	A28	D0:3	DL28
A0:2	A29	D0:2	DL29
A0:1	A30	D0:1	DL30
A0:0	A31	D0:0	DL31
C3:7	TT3	C1:7	TRST* (603 and 604) †
C3:6	TT2	C1:6	TMS (603 and 604) †
C3:5	TEA*‡	C1:5	TDO (603 and 604) †
C3:4	BG*	C1:4	TDI (603 and 604) †

Table 1–5: 192-channel: PowerPC 60X connections for the LO module (cont.)

Section: channel	Connect to PPC60X signal	Section: channel	Connect to PPC60X signal
C3:3	TSIZ2	C1:3	CKSTP_OUT*= (603 and 604) †
C3:2	TBST*	C1:2	CKSTP_IN*= (603 and 604) †
C3:1	TT0	C1:1	MPC* (603 and 604) †
C3:0	XATS*§	C1:0	SMI* (603 and 604) †
C2:7	TSIZ1	C0:7	TC2 (604) †
C2:6	TSIZ0	C0:6	HALTED (604) †
C2:5	DBB*¶	C0:5	ARRAY_WR* (604) †
C2:4	ABB*	C0:4	RUN (604) †
C2:3	XATS*§	C0:3	LSSD_MODE* (603 and 604) †
C2:2	TS*#	C0:2	L1_TSTCLK (603 and 604) †
C2:1	AACK*%	C0:1	L2_TSTCLK (603 and 604) †
C2:0	ARTRY*@	C0:0	Not connected

† **Not required for disassembly.**

‡ **TEA* is also probed by HI_CLK:0 and LO_CLK:0.**

§ **XATS* is also probed by HI_C2:3.**

¶ **DBB* is also probed by HI_CLK:2 and LO_CLK:2.**

\# **TS* is also probed by HI_C2:2.**

% **AACK* is also probed by HI_C2:1.**

@ **ARTY* is also probed by HI_C2:0, and HI_C3:6.**

Table 1–6 shows the PowerPC 60X signals to which the clock channels must connect for disassembly to be correct.

Table 1–6: PowerPC 60X connections for the clock channels

136-channel section & probe	192-channel section & probe	Clock or Qual	PowerPC 60X signal name	
CK:3	HI_CK:3, LO_CK:3	Clock (rising edge)	SYSCLK=	(SYSCLK)†
CK:2	HI_CK:2, LO_CK:2	Qual	DBB*=	(DBB*)
CK:1	HI_CK:1, LO_CK:1	Qual	TA*=	(TA*)
CK:0	HI_CK:0, LO_CK:0	Qual	TEA*=	(TEA*)

† **In a 601 SUT, connect the SYSCLK= signal to a 1X clock (such as the BCLK_EN* signal). Refer to *Requirements and Restrictions* in the *Getting Started* chapter for more detailed information on this clock.**

6. Align pin 1 of your test clip with the corresponding pin 1 of the microprocessor in your SUT and attach it to the microprocessor.

Refer to the channel assignment tables in the *Specifications* chapter to see the signal-to-channel assignments.

Applying and Removing Power

A power supply for the PowerPC 60X probe adapter is included with the support. The power supply provides +5 volts power to the probe adapter. The center connector of the power jack connects to Vcc.

NOTE. *Whenever the SUT is powered off, be sure to remove power from the probe adapter.*

To apply power to the PowerPC 60X probe adapter and SUT, follow these steps:

1. Measure the resistance between Vcc and ground to verify that they are not shorted together.

   If you detect a short, determine the source and repair the problem before applying power.

CAUTION. *Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and PowerPC 60X microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

2. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–9 shows the location of the jack on the adapter board.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the PowerPC 60X microprocessor and SUT.*

3. Plug the power supply for the probe adapter into an electrical outlet. When power is present on the probe adapter, an LED lights near the power jack.
4. Power on the SUT.

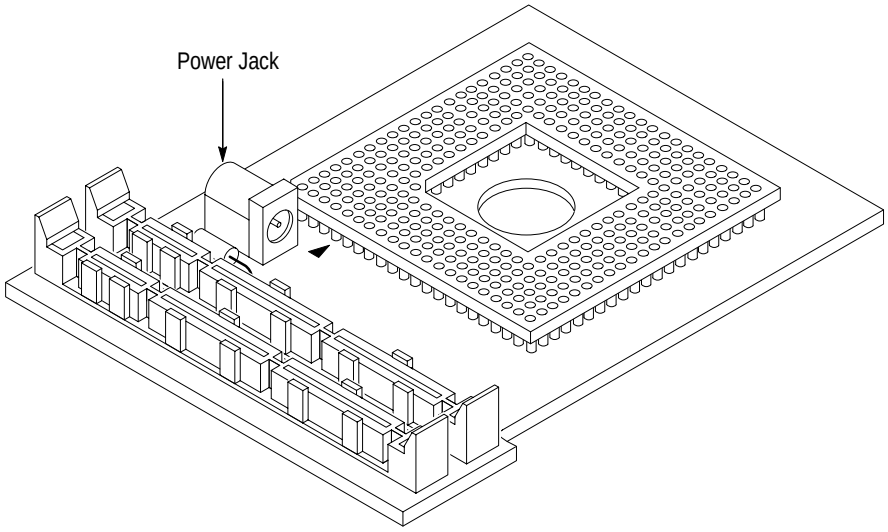


Figure 1–9: Location of the power jack

To remove power from the SUT and PowerPC 60X probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the PowerPC 60X microprocessor and SUT.*

1. Power off the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 540 PowerPC 60X support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the PowerPC 60X microprocessor are Address, Hi_Data, Lo_Data, Control, Transfer, Tsiz, Com_60X, PPC601_4, PPC603_4 , PPC604, Misc, and Clock. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–4.

Clocking Options

The TMS 540 support offers a microprocessor-specific clocking mode for the PowerPC 60X microprocessor. This clocking mode is the default selection whenever you load the PPC60X support.

NOTE*. For the PPC601 microprocessor, you might not acquire correct data when you connect the HI:CK3 and LO:CK3 channels to the BCLK_EN* signal. Refer to the description of the PPC601 SYSCLK signal under* Requirements and Restrictions *in the* Getting Started *chapter.*

A description of how cycles are sampled by the module using the TMS 540 support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

NOTE. *An earlier version of this software had a clocking option in which you could acquire data with Joined Address and Data, or Separated Address and Data. Although this clocking option is no longer available, you can still use this software to view data acquired with Joined or Separated address and data.*

The clocking option for the TMS 540 application is DRTRY Cycles.

DRTRY Cycles You can include or exclude DRTRY Cycles. These types of cycles are acquired when you select Included.

You must select to always acquire data after the TA signal goes true to test for the DRTRY signal, or to skip the sample unless some other important signals are valid at that time. If you include DRTRY cycles, and there is no DRTRY cycle or no other valid informationat this time, then the cycle is labeled (UNKNOWN).

Symbols

The TMS 540 application supplies three symbol table files. The symbol table file replaces specific channel group values with symbolic values when the group is displayed symbolically.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the Control channel group symbol table. The Control group symbol table file name is PPC60X_Ctrl.

Table 2–1: Control group symbol table definitions

Symbol	Control group value				Meaning
	XATS_B2* TS* XATS* BG*	DBG* ARTRY* DRTRY* AACK*	ARTRY_ERLY* DRTRY_ERLY* TA* TEA*	ARTRY_DATA* ABB* DBWO* DBB*	
ART_M0E	X X X X	0 0 X X	X X X 0	X X X X	ARTRY cycle and MPC0's Data Error
ART_M1E	X X X X	X 0 X X	X X X 0	X X X X	ARTRY cycle and MPC1's Data Error
ART_DRT	X X X X	X 0 0 X	X X X X	X X X X	ARTRY cycle and Data Retry
ART_M0D	X X X X	0 0 X X	X X 0 X	X X X X	ARTRY cycle and MPC0's Data
ART_M1D	X X X X	X 0 X X	X X 0 X	X X X X	ARTRY cycle and MPC1's Data
M0A_M0E	1 0 1 0	0 1 X X	X X X 0	X X X X	MPC0's Address and MPC0's Data Error
M0P0_M0E	1 1 0 0	0 1 X X	X X X 0	X X X X	MPC0's DSA packet 0 and MPC0's Data Error
M0P1_M0E	0 1 1 0	0 1 X X	X X X 0	X X X X	MPC0's DSA packet 1 and MPC0's Data Error
M0A_M1E	1 0 1 0	X 1 X X	X X X 0	X X X X	MPC0's Address and MPC1's Data Error
M0P0_M1E	1 1 0 0	X 1 X X	X X X 0	X X X X	MPC0's DSA packet 0 and MPC1's Data Error
M0P1_M1E	0 1 1 0	X 1 X X	X X X 0	X X X X	MPC0's DSA packet 1 and MPC1's Data Error
M1A_M0E	1 0 1 X	0 1 X X	X X X 0	X X X X	MPC1's Address and MPC0's Data Error
M1P0_M0E	1 1 0 X	0 1 X X	X X X 0	X X X X	MPC1's DSA packet 0 and MPC0's Data Error
M1P1_M0E	0 1 1 X	0 1 X X	X X X 0	X X X X	MPC1's DSA packet 1 and MPC0's Data Error
M1A_M1E	1 0 1 X	X 1 X X	X X X 0	X X X X	MPC1's Address and MPC1's Data Error
M1P0_M1E	1 1 0 X	X 1 X X	X X X 0	X X X X	MPC1's DSA packet 0 and MPC1's Data Error
M1P1_M1E	0 1 1 X	X 1 X X	X X X 0	X X X X	MPC1's DSA packet 1 and MPC1's Data Error
M0A_DRT	1 0 1 0	X 1 0 X	X X X X	X X X X	MPC0's Address and Data retry
M0P0_DRT	1 1 0 0	X 1 0 X	X X X X	X X X X	MPC0's DSA packet 0 and Data retry
M0P1_DRT	0 1 1 0	X 1 0 X	X X X X	X X X X	MPC0's DSA packet 1 and Data retry
M1A_DRT	1 0 1 X	X 1 0 X	X X X X	X X X X	MPC1's Address and Data retry
M1P0_DRT	1 1 0 X	X 1 0 X	X X X X	X X X X	MPC1's DSA packet 0 and Data retry
M1P1_DRT	0 1 1 X	X 1 0 X	X X X X	X X X X	MPC1's DSA packet 1 and Data retry
M0A_M0D	1 0 1 0	0 1 X X	X X X X	X X 0 X	MPC0's Address and Data
M0P0_M0D	1 1 0 0	0 1 X X	X X 0 X	X X X X	MPC0's DSA packet 0 and Data
M0P1_M0D	0 1 1 0	0 1 X X	X X 0 X	X X X X	MPC0's DSA packet 1 and Data
M0A_M1D	1 0 1 0	X 1 X X	X X 0 X	X X X X	MPC0's Address and MPC1's Data
M0P0_M1D	1 1 0 0	X 1 X X	X X 0 X	X X X X	MPC0's DSA packet 0 and MPC1's Data
M0P1_M1D	0 1 1 0	X 1 X X	X X 0 X	X X X X	MPC0's DSA packet 1 and MPC1's Data
M1A_M0D	1 0 1 X	0 1 X X	X X 0 X	X X X X	MPC1's Address and MPC0's Data
M1P0_M0D	1 1 0 X	0 1 X X	X X 0 X	X X X X	MPC1's DSA packet 0 and MPC0's Data
M1P1_M0D	0 1 1 X	0 1 X X	X X 0 X	X X X X	MPC1's DSA packet 1 and MPC0's Data

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value XATS_B2* TS* XATS* BG* / DBG* ARTRY* DRTRY* AACK* / ARTRY_ERLY* DRTRY_ERLY* TA* TEA* / ARTRY_DATA* ABB* DBWO* DBB*	Meaning
M1A_M1D	1 0 1 X / X 1 X X / X X 0 X / X X X X	MPC1's Address and Data
M1P0_M1D	1 1 0 X / X 1 X X / X X 0 X / X X X X	MPC1's DSA packet 0 and Data
M1P1_M1D	0 1 1 X / X 1 X X / X X 0 X / X X X X	MPC1's DSA packet 1 and Data
M0_A	1 0 1 0 / X 1 X X / X X X X / X X X X	MPC0's Address cycle
M0_P0	1 1 0 0 / X 1 X X / X X X X / X X X X	MPC0's DSA packet 0 cycle
M0_P1	0 1 1 0 / X 1 X X / X X X X / X X X X	MPC0's DSA packet 1 cycle
M1_A	1 0 1 X / X 1 X X / X X X X / X X X X	MPC1's Address cycle
M1_P0	1 1 0 X / X 1 X X / X X X X / X X X X	MPC1's DSA packet 0 cycle
M1_P1	0 1 1 X / X 1 X X / X X X X / X X X X	MPC1's DSA packet 1 cycle
M0_E	X X X X / 0 X X X / X X X 0 / X X X X	MPC0's Data Error
M1_E	X X X X / X X X X / X X X 0 / X X X X	MPC1's Data Error
DRT	X X X X / X X 0 X / X X X X / X X X X	DRTRY cycle
M0_D	X X X X / 0 X X X / X X 0 X / X X X X	MPC0's Data cycle
M1_D	X X X X / X X X X / X X 0 X / X X X X	MPC1's Data cycle
ART	X X X X / X 0 X X / X X X X / X X X X	ARTRY cycle
UNKNOWN	X X X X / X X X X / X X X X / X X X X	Unknown cycle

Table 2–2 shows the name, bit pattern, and meaning for the symbols in the Transfer channel group symbol table. The Transfer group symbol table file name is PPC60X_Trans.

Table 2–2: Transfer group symbol table definitions

Symbol	Transfer group value TT0 TT1 TT2 TT3 / TC0 GBL*	Meaning
FETCH	X 1 X 1 / 1 X	Instruction Fetch cycle
READ	X 1 X 1 / 0 X	Data Read cycle
WRITE	X 0 X 1 / X X	Data Write cycle
ADDR_ONLY	X X X 0 / X X	Address only cycle
UNKNOWN	X X X X / X X	Unknown cycle

Table 2–3 shows the name, bit pattern, and meaning for the symbols in the the Transfer Size channel group symbol table. The Transfer Size group symbol table file name is PPC60X_Tsiz.

Table 2–3: Transfer Size group symbol table definitions

Symbol	Transfer Size group value TSIZ0 TSIZ1 TSIZ2 TBST*	Meaning
BURST	0 1 0 0	Burst transfer
8BYTE	0 0 0 1	Eight byte transfer
4BYTE	1 0 0 1	Four byte transfer
2BYTE	0 1 0 1	Two byte transfer
1BYTE	0 0 1 1	One byte transfer
UNKNOWN	X X X X	Unknown transfer size

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the PPC60X support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–13.*

The default display format shows the Address, Data, Control, Transfer, and Tsiz channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 shows these special characters and strings, and gives a definition of what they represent.

Table 2–4: Meaning of special characters in the display

Character or string displayed	Meaning
≫ or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
--------	In the Address channel group, this indicates that the Data group did not have information that could be disassembled
--------	In the HI_Data and LO_Data groups, this indicates that the sequence does not contain valid data
--------	In the LO_Data group, indicates that the bus configuration is 32-Bits
--	In the invalidate byte lanes, this indicates a Data Read or Data Write transaction
--------	Indicates a flushed instruction when the microprocessor is operating in 64-bit mode and only one of the instructions fetched is executed
<Hex value>	In whole bytes that are not valid, indicates invalidated data; the value for invalidated data is hexcadecimal

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses.

If a single sequence has both an Address/Direct Store Access cycle and a Data cycle, then a combination of cycle type labels described in Tables 2–5, 2–6, and 2–7 are displayed. For example, if Alternate Master Address and Alternate Master Data are acquired in one sample, the disassembler would display the cycle type label (ALT ADDRS AND ALT DATA).

Table 2–5 shows cycle type labels for Address sequences, and gives a definition of the cycle they represent.

Table 2–5: Cycle type labels for Address sequences and definitions

Cycle type label	Definition
(60X_ADDRS)	Address cycle with selected PPC60X master
(60X_ART_ADDRS)	Selected PPC60X Address retried
(ALT_ADDRS)	Alternate masters address
(INCOM_ADDRS)	Invalid selected PPC60X Address which is not associated with its data

Table 2–6 shows cycle type labels for Direct Store Access sequences, and gives a definition of the cycle they represent.

Table 2–6: Cycle type labels for Direct Store Access sequences and definitions

Cycle type label	Definition
(LOAD START)	Request for I/O load operations
(LOAD IMMEDIATE)	Transfer of up to 32 bits of data from the Bus Unit Controller to the selected PPC60X
(LOAD LAST)	Transfer of last 32 bits of data from the Bus Unit Controller to the selected PPC60X
(STORE IMMEDIATE)	Transfer of up to 32 bits of data from the selected PPC60X to the Bus Unit Controller
(STORE LAST)	Transfer of last 32 bits of data from the selected PPC60X to the Bus Unit Controller
(LOAD REPLY)	Reply from the Bus Unit Controller to indicate the success or failure of an I/O load operation
(STORE REPLY)	Reply from the Bus Unit Controller to indicate the success or failure of an I/O store operation
(UNKNOWN DSA)	Unrecognized I/O operation
(60X_PKT1 XATC=0x$$)	Selected PPC60X Direct Store Access Packet 1 with XATC in Hex
(60X_ART_DSA)	Direct Store Access retried
(ALT_PKT0)	Alternate Masters Direct Store Access packet 0
(ALT_PKT1)	Alternate Masters Direct Store Access packet 1

Table 2–7 shows cycle type labels for Data sequences, and gives a definition of the cycle they represent.

Table 2–7: Cycle type labels for Data sequences and definitions

Cycle type label	Definition
(60X_DATA)	Data cycle with selected PPC60X master
(ALT_DATA)	Alternate masters data
(60X_DRT_DATA)	Selected PPC60X Data retried
(INCOM_DATA)	Invalid selected PPC60X Data which is not associated with its address
(60X_DSA_DATA)	Selected PPC60X Direct Storage Access Data

Table 2–8 shows cycle type labels for ARTRY, DRTRY, and Data Error cycles, and gives a definition of the cycle they represent.

Table 2–8: Cycle type labels for ARTRY, DRTRY, and Data Error cycles

Cycle type label	Definition
(DATA_RETRY)	Sequence with the DRTRY* signal asserted
(60X_DATA_ERR)	Data error in the selected PPC60X data; the TEA* signal is asserted
(ALT_DATA_ERR)	Data error in Alternate masters data
(ARTRY_CYCLE)	Sequence with the ARTRY* signal asserted
(UNKNOWN)*	Cycle with out valid information

*** If acquired with the DRTRY Included clocking option, the cycle following a valid data cycle is always acquired in anticipation of a Data retry. If that cycle does not have any valid information, the cycle is not displayed.**

Table 2–9 shows cycle type labels for general cycle types (not sequence types), and gives a definition of the cycle they represent.

Table 2–9: General cycle type labels definitions

Cycle type label	Definition
(FLUSH)	An instruction that was fetched but not executed
(FLUSH: PREDICTION FAIL)	An instruction that was fetched based on the prediction bit, but the prediction bit was incorrect
(CACHE FILL)	Burst read transfer that occurrs after the wrap around of the end of the cache line
(CLEAN BLOCK)	Clean Block transaction
(WRT WITH FLUSH)	Write-with-Flush operation issued by the microprocessor
(FLUSH BLOCK)	Flush Block transaction
(WRT WITH KILL)	Write-with-Kill transaction
(SYNC)	Address Only transaction due to the execution of Sync instruction
(DATA READ)	Single Beat Read or Burst Read operation
(KILL BLOCK)	Kill Block transaction
(RWITM)	Read-with-Intent-to-Modify transaction
(ORD I/O OPRN)	Ordered I/O operation
(WWF-ATOMIC)	Write-with-Flush-Atomic operation issued by the microprocessor
(EXT CTR WD WRT)	External Control Word Write transaction
(TLB INVAL)	TLB invalidate transaction issued by the microprocessor

Table 2–9: General cycle type labels definitions (cont.)

Cycle type label	Definition
(READ-ATOMIC)	Read-Atomic operation
(EXT CTR WD RD)	External Control Word Read transaction
(RWITM-ATOMIC)	Read-with-Intent-to-Modify-Atomic transaction
(RESVD)	Reserved-with-Intent-to-Modify transaction type
(**BAD CYCLE TYPE**)	Cycle type where the value in the Trans group does not match any of the defined patterns

Figure 2–1 shows an example of disassembled PPC60X data in the Hardware display format.

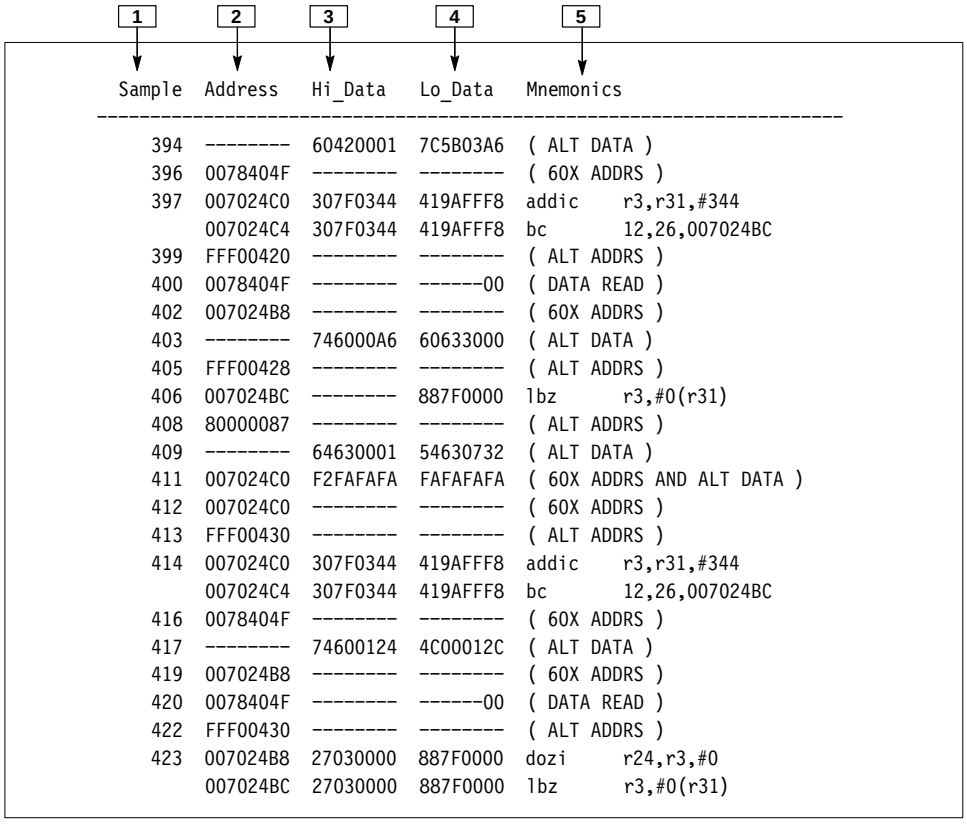


Figure 2–1: Disassembled data in the Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the PowerPC 60X address bus.

3 **Hi_Data Group.** Lists data from channels connected to the PowerPC 60X DH31-DH0 signals.

4 **Lo_Data Group.** Lists data from channels connected to the PowerPC 60X DL31-DL0 signals.

5 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the PowerPC 60X microprocessor are as follows:

b	bl	sc
ba	bla	rfi

Instructions that might generate a change in the flow of control in the PowerPC 60X microprocessor are as follows:

bc	bcla	bcctr	tdi
bca	bclr	bcctrl	tw
bcl	bclrl	td	twi

The disassembler displays some instructions that cause traps or interrupts, as well as exception vector reads that are taken and `( **BAD CYCLE TYPE** )`. Mnemonics misinterpreted by the disassembler are also displayed.

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the PowerPC 60X microprocessor are as follows:

sc	rfi

Instructions that might generate a subroutine call or a return in the PowerPC 60X microprocessor are as follows:

td	tdi	tw	twi

The disassembler displays some instructions that cause traps or interrupts, as well as exception vector reads that are taken and `( **BAD CYCLE TYPE** )`. Mnemonics misinterpreted by the disassembler are also displayed.

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the PowerPC 60X support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Select a bus configuration and the trace PPC60X microprocessor
- Select the prefetch byte order
- Select the alternate byte order low and high bounds
- Select the exception byte order
- Specify the exception prefix

You can include or exclude DRTRY cycles in the acquisition through the DRTRY Cycles clocking option.

The PowerPC 60X microprocessor support product has six additional fields: Bus Config/Proc Select, Prefetch Byte Ord, Alt-Byte Ord - Lo Bound, Alt-Byte Ord - Hi Bound, Exception Byte Ord, and Exception Prefix. These fields appear in the area indicated in the basic operations user manual.

Bus Config/Proc Select. The PPC60X microprocessor can support optional configurations that are selected by the DRTRY*, TLBISYNC*, and QACK* signals when the HRESET* is deasserted after you start the system.

You should select the bus configuration that matches the one in your PPC60X-based system: 64-bit Data bus, or 32-Bit Data bus.

You can use either 64-bit configuration when your SUT is operating in 64–bit mode. This is the default bus configuration.

You can also use either 32-Bit Data Bus configuration when your SUT is operating in 32-bit mode. With this configuration, only the Hi_Data channels corresponding to the DH31-DH0 signals are valid.

You can also select which PPC60X microprocessor to trace: MPC0 or MPC1. The MPC0 is considered to be the microprocessor from which the BG* and DBG* signals are acquired. All other microprocessors, including controllers, are considered to be MPC1s.

Prefetch Byte Ord. You can select the byte ordering for the predominant instruction fetches as Big- or Little-Endian.

Alt Byte Ord - Lo Bound and Alt Byte Ord - Hi Bound. You can enter the low and high bounds for the alternate byte ordering range. The default is 00000000.

You should enter alternate values on double-word boundaries. If the value is not on a double-word boundary, the disassembler assumes the value to be the nearest double-word.

If you do not enter a value in the field, the data is acquired and disassembled according to the selection in the Prefetch Byte Ord field.

NOTE*. The alternate high bound value must be greater than the alternate low bound value or disassembly will be incorrect.*

Exception Byte Ord. You can select the byte ordering for exception processing as Big- or Little-Endian.

Exception Prefix. You can enter the prefix value of the exception table as 000 to FFF. The default prefix value is FFF. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

NOTE*. If an address is in the Exception processing region and in the range selected for the alternate byte ordering, the disassembler uses the byte ordering selected for the Exception processing.*

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

The list of selections varies depending on the selection in the Bus Config/Proc Select field in the Disassembly property page (Disassembly Format Definition overlay).

Mark selections available on data sequences without an address and data cycle associated with a fetch cycle when the PPC60X microprocessor is operating in 64-bit mode are as follows:

```
Opcode                          Opcode
Opcode                          Flush
Flush                           Opcode
Flush                           Flush
Incom_Data
Undo Mark
```

Mark selections available on data sequences without an address and data cycle associated with a fetch cycle when the PPC60X microprocessor is operating in 32-bit mode are as follows:

```
Opcode
Flush
Incom_Data
Undo Mark
```

Mark selections available on sequences with only an Address cycle are as follows:

```
Incom_Address
Undo Mark
```

Mark selections available on sequences with both data and address cycles (if the data cyle is associated with a fetch cycle) and the PPC60X microprocessor is operating in 64-bit mode are as follows:

```
Opcode                          Opcode
Opcode                          Flush
Flush                           Opcode
Flush                           Flush
Incom_Data
Incom_Address
Opcode                          Opcode Incom_Addrs
Opcode                          Flush Incom_Addrs
Flush                           Opcode Incom_Addrs
Flush                           Flush Incom_Addrs
Incom_Data Incom_Addrs
Undo Mark
```

Mark selections available on sequences with both data and address cycles (if the data cyle is associated with a fetch cycle) and the PPC60X microprocessor is operating in 32-bit mode are as follows:

```
Opcode
Flush
Incom_Data
Incom_Address
Opcode Incom_Addrs
Flush Incom_Addrs
Incom_Data Incom_Addrs
Undo Mark
```

Mark selections available on sequences with data that is not associated with a Fetch cycle are as follows:

```
Incom_Data
Undo Mark
```

Table 2–10 describes the various combinations of mark selections.

Table 2–10: Mark selections and definitions

Mark selection or combination†		Definition
Opcode	Opcode	HI_Data and LO_Data are disassembled
Opcode	Flush	Only HI_Data is disassembled in Big-Endian mode or only LO_Data is disassembled in Little-Endian mode
Flush	Opcode	Only LO_Data is disassembled in Big-Endian mode or only HI_Data is disassembled in Little-Endian mode
Flush	Flush	Instructions not disassembled and labeled as (FLUSH)
Incom_Addrs		Valid PPC60X address is invalidated and labeled as (Incom_Addrs)
Opcode	Opcode Incom_Addrs	Use to mark a sequence with PPC60X address and data from different transactions; HI_Data and LO_Data are disassembled; the address is invalidated
Opcode	Flush Incom_Addrs	HI_Data is disassembled only in Big-Endian mode or LO_Data is disassembled only in Little-Endian mode; the address is invalidated
Flush	Opcode Incom_Addrs	LO_Data is disassembled only in Big-Endian mode or HI_Data is disassembled only in Little-Endian mode; the address is invalidated
Flush	Flush Incom_Addrs	Instructions not disassembled and labeled as (FLUSH); the address is invalidated
Opcode		HI_Data and LO_Data are disassembled
Flush		HI_Data and LO_Data are not disassembled and labeled as (FLUSH)
Incom_Addrs		Address is invalidated
Opcode Incom_Addrs		HI_Data and LO_Data are disassembled; the address is invalidated
Flush Incom_Addrs		HI_Data and LO_Data are not disassembled and labeled as (FLUSH); the address is invalidated

Table 2–10: Mark selections and definitions (cont.)

Mark selection or combination†	Definition
`Incom_Data`	HI_Data and LO_Data are invalidated
`Incom_Addrs Incom_Data`	Address, HI_Data, and LO_Data are invalidated
`Undo Mark`	Removes all marks

† **Mark selections intended to be used on sequences with data are not available for non-instructions.**

The Incom_Addrs mark invalidates the address from being associated with the wrong data. You can use this mark if you determine that the data for the address was not acquired.

The Incom_Data mark invalidates the data from being associated with the wrong address. You can use this mark if you determine that the address for the data was not acquired.

Information on basic operations contains more details on marking cycles.

Displaying Exception Labels

The disassembler can display PowerPC 60X exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

You can enter the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the offset address; enter a three-digit hexadecimal value corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–11 lists the PowerPC 60X interrupt and exception labels.

Table 2–11: Interrupt and exception labels

Exception number	Offset	Displayed interrupt or exception name
0	0x00000	(RESERVED)
1	0x00100	(SYSTEM RESET)
2	0x00200	(MACHINE CHECK)
3	0x00300	(DSI)
4	0x00400	(ISI)
5	0x00500	(EXTERNAL INTERRUPT)
6	0x00600	(ALIGNMENT)
7	0x00700	(PROGRAM)

Table 2–11: Interrupt and exception labels (cont.)

Exception number	Offset	Displayed interrupt or exception name
8	0x00800	(FLOATING-POINT UNAVAILABLE)
9	0x00900	(DECREMENTER)
10	0x00A00	(RESERVED)
11	0x00B00	(RESERVED)
12	0x00C00	(SYSTEM CALL)
13	0x00D00	(TRACE)
14	0x00E00	(FLOATING-POINT ASSIST)
15	0x00F00	(PERF MONITORING INTRPT)
16	0x01000	(INST TRANS MISS)
17	0x01100	(DATA LOAD TRANS MISS)
18	0x01200	(DATA TRANS MISS)
19	0x01300	(INST ADDRESS BREAKPOINT)
20	0x01400	(SYS MANAGEMENT INTERRUPT)
21-32	0x014FF to 0x02FFF	(RESERVED)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your PowerPC 60X microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires PowerPC 60X signals
- List of other accessible microprocessor signals and extra probe channels
- Alphabetical list of signal names mapped to the PGA socket pin numbers for each type of PowerPC 60X microprocessor supported

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a PowerPC 60X microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

Table 1–1 in the *Getting Started* chapter shows which microprocessors and their packages the TMS 540 supports.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data. Table 3–2 shows the environmental specifications. Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–1: Electrical specifications

Characteristics	Requirements	
Probe adapter power supply requirements		
Voltage	90-265 VAC	
Current	1.1 A maximum at 100 VAC	
Frequency	47-63 Hz	
Power	25 W maximum	
SUT clock		
Clock rate	Max. 66 MHz	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
SYSCLK, DBB*, TA*, TEA*, XATS*, ARTRY*, DRTRY*	21 pF	2 @ 74FCT162244ET
Remaining signals	14 pF	74FCT162244ET

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed PowerPC 60X microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter. The figure also shows the minimum vertical clearance of the high-density probe cable.

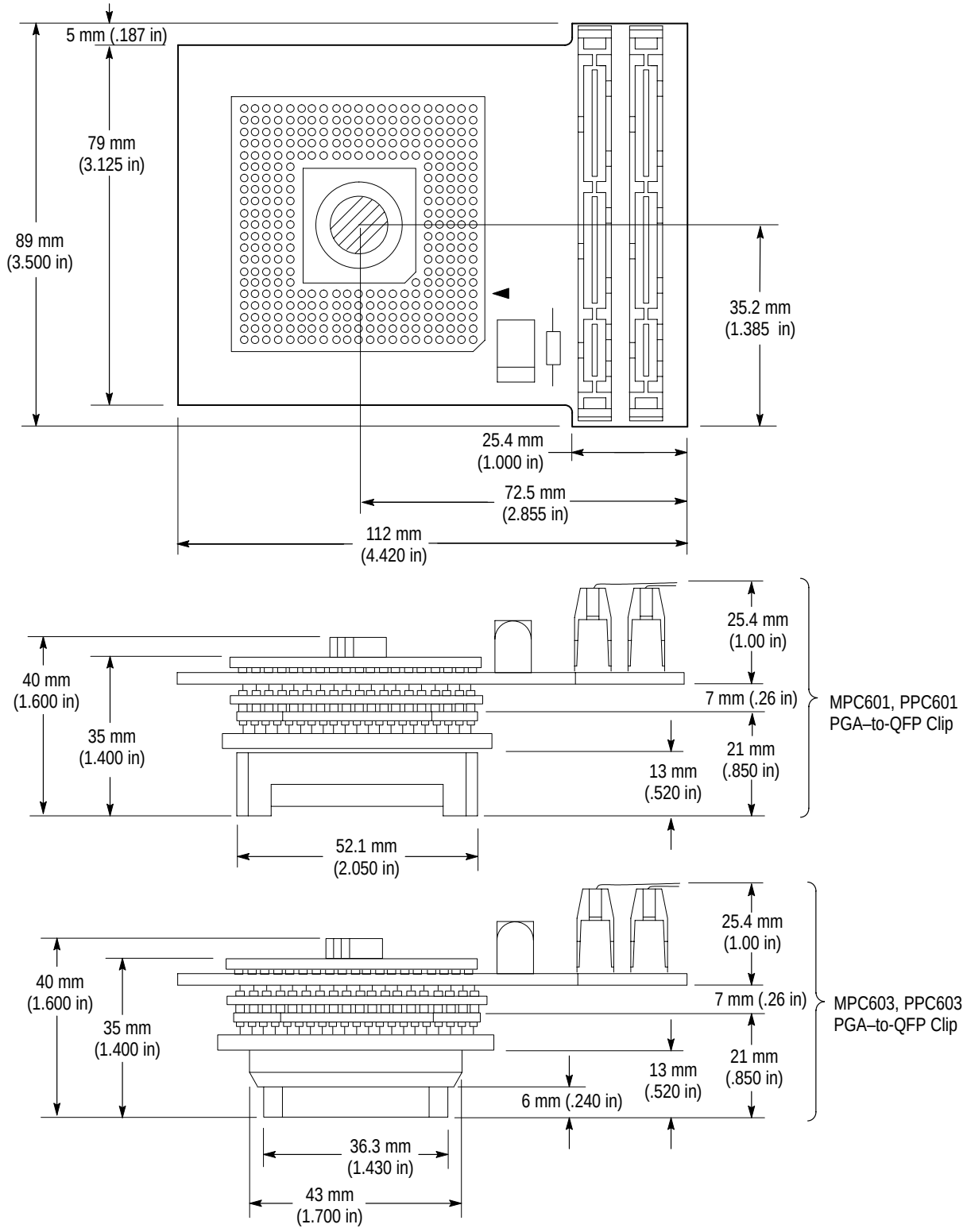


Figure 3–1: Dimensions of the probe adapter and converter clips

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–15 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.
- For the 192-channel module, the module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

Table 3–4 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. The default display radix is HEX.

Table 3–4: Address group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
31	A3:7	LO_A3:7	A0
30	A3:6	LO_A3:6	A1
29	A3:5	LO_A3:5	A2
28	A3:4	LO_A3:4	A3
27	A3:3	LO_A3:3	A4
26	A3:2	LO_A3:2	A5
25	A3:1	LO_A3:1	A6
24	A3:0	LO_A3:0	A7
23	A2:7	LO_A2:7	A8
22	A2:6	LO_A2:6	A9
21	A2:5	LO_A2:5	A10
20	A2:4	LO_A2:4	A11
19	A2:3	LO_A2:3	A12
18	A2:2	LO_A2:2	A13
17	A2:1	LO_A2:1	A14
16	A2:0	LO_A2:0	A15
15	A2:7	LO_A1:7	A16
14	A1:6	LO_A1:6	A17
13	A1:5	LO_A1:5	A18
12	A1:4	LO_A1:4	A19
11	A1:3	LO_A1:3	A20
10	A1:2	LO_A1:2	A21
9	A1:1	LO_A1:1	A22
8	A1:0	LO_A1:0	A23
7	A0:7	LO_A0:7	A24
6	A0:6	LO_A0:6	A25
5	A0:5	LO_A0:5	A26
4	A0:4	LO_A0:4	A27
3	A0:3	LO_A0:3	A28
2	A0:2	LO_A0:2	A29
1	A0:1	LO_A0:1	A30
0	A0:0	LO_A0:0	A31

Table 3–5 shows the probe section and channel assignments for the Hi_Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Hi_Data group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
31	E3:7	HI_A3:7	DH0
30	E3:6	HI_A3:6	DH1
29	E3:5	HI_A3:5	DH2
28	E3:4	HI_A3:4	DH3
27	E3:3	HI_A3:3	DH4
26	E3:2	HI_A3:2	DH5
25	E3:1	HI_A3:1	DH6
24	E3:0	HI_A3:0	DH7
23	E2:7	HI_A2:7	DH8
22	E2:6	HI_A2:6	DH9
21	E2:5	HI_A2:5	DH10
20	E2:4	HI_A2:4	DH11
19	E2:3	HI_A2:3	DH12
18	E2:2	HI_A2:2	DH13
17	E2:1	HI_A2:1	DH14
16	E2:0	HI_A2:0	DH15
15	E1:7	HI_A1:7	DH16
14	E1:6	HI_A1:6	DH17
13	E1:5	HI_A1:5	DH18
12	E1:4	HI_A1:4	DH19
11	E1:3	HI_A1:3	DH20
10	E1:2	HI_A1:2	DH21
9	E1:1	HI_A1:1	DH22
8	E1:0	HI_A1:0	DH23
7	E0:7	HI_A0:7	DH24
6	E0:6	HI_A0:6	DH25
5	E0:5	HI_A0:5	DH26
4	E0:4	HI_A0:4	DH27
3	E0:3	HI_A0:3	DH28
2	E0:2	HI_A0:2	DH29
1	E0:1	HI_A0:1	DH30
0	E0:0	HI_A0:0	DH31

Table 3–6 shows the probe section and channel assignments for the Lo_Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Lo_Data group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
31	D3:7	LO_D3:7	DL0
30	D3:6	LO_D3:6	DL1
29	D3:5	LO_D3:5	DL2
28	D3:4	LO_D3:4	DL3
27	D3:3	LO_D3:3	DL4
26	D3:2	LO_D3:2	DL5
25	D3:1	LO_D3:1	DL6
24	D3:0	LO_D3:0	DL7
23	D2:7	LO_D2:7	DL8
22	D2:6	LO_D2:6	DL9
21	D2:5	LO_D2:5	DL10
20	D2:4	LO_D2:4	DL11
19	D2:3	LO_D2:3	DL12
18	D2:2	LO_D2:2	DL13
17	D2:1	LO_D2:1	DL14
16	D2:0	LO_D2:0	DL15
15	D1:7	LO_D1:7	DL16
14	D1:6	LO_D1:6	DL17
13	D1:5	LO_D1:5	DL18
12	D1:4	LO_D1:4	DL19
11	D1:3	LO_D1:3	DL20
10	D1:2	LO_D1:2	DL21
9	D1:1	LO_D1:1	DL22
8	D1:0	LO_D1:0	DL23
7	D0:7	LO_D0:7	DL24
6	D0:6	LO_D0:6	DL25
5	D0:5	LO_D0:5	DL26
4	D0:4	LO_D0:4	DL27
3	D0:3	LO_D0:3	DL28
2	D0:2	LO_D0:2	DL29
1	D0:1	LO_D0:1	DL30
0	D0:0	LO_D0:0	DL31

Table 3–7 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: Control group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
15	C3:0	LO_C3:0	XATS_B2* (Delayed XATS*)
14	C2:2	LO_C2:2	TS*
13	C2:3	LO_C2:3	XATS*
12	C3:4	LO_C3:4	BG*
11	C1:4	HI_C3:4	DBG*
10	C1:6	HI_C3:6	ARTRY*
9	C1:2	HI_C3:2	DRTRY*
8	C2:1	LO_C2:1	AACK*
7	C2:0	LO_C2:0	ARTRY_ERLY* (ARTRY* sampled early to determine bus master)
6	C1:0	HI_C3:0	DRTRY_ERLY* (DRTRY* sampled early to determine bus master)
5	C0:6	HI_C2:6	TA*
4	C3:5	LO_C3:5	TEA*
3	C0:0	HI_C2:0	ARTRY_DATA* (ARTRY* sampled before TA* to determine bus master)
2	C2:4	LO_C2:4	ABB*
1	C0:4	HI_C2:4	DBWO*
0	C2:5	LO_C2:5	DBB*

Table 3–8 shows the probe section and channel assignments for the Transfer group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: Transfer group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
5	C3:1	LO_C3:1	TT0
4	C0:7	HI_C2:7	TT1
3	C3:6	LO_C3:6	TT2
2	C3:7	LO_C3:7	TT3
1	C1:7	HI_C3:7	TC0
0	C0:5	HI_C2:5	GBL*

Table 3–9 shows the probe section and channel assignments for the Tsiz group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Tsiz group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
3	C2:6	LO_C2:6	TSIZ0
2	C2:7	LO_C2:7	TSIZ1
1	C3:3	LO_C3:3	TSIZ2
0	C3:2	LO_C3:2	TBST*

Table 3–10 shows the probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Misc group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	PowerPC 60X signal name
2	C1:1	HI_C3:1	HRESET*†
1	C1:3	HI_C3:3	SYSCLK†
0	C1:5	HI_C3:5	BR_SHD*†‡

† **Signal not required for disassembly.**

‡ **BR* signal on the PPC603 microprocessor; SHD* signal on the PPC601 microprocessor.**

Table 3–11 shows the probe section and channel assignments for the Com_60X group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–11: 192-channel: Com_60X group channel assignments

Bit order	Section & probe	PowerPC 60X signal name
20	HI_D3:7	DPE*†
19	HI_D3:6	DP7†
18	HI_D3:5	DP6†
17	HI_D3:4	DP5†
16	HI_D3:3	DP4†
15	HI_D3:2	DP3†
14	HI_D3:1	DP2†
13	HI_D3:0	DP1†
12	HI_D2:7	DP0†
11	HI_D2:6	RSRV*†
10	HI_D2:5	TC1†
9	HI_D2:4	WT*†
8	HI_D2:3	TT4†
7	HI_D2:2	SRESET*†
6	HI_D2:1	INT*†
5	HI_D2:0	APE*†
4	HI_D1:7	AP3†
3	HI_D1:6	AP2†
2	HI_D1:5	AP1†
1	HI_D1:4	AP0†
0	HI_D1:3	CI*†

† **Signal not required for disassembly.**

Table 3–12 shows the probe section and channel assignments for the PPC601_4 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–12: 192-channel: PPC601_4 group channel assignments

Bit order	Section & probe	PowerPC 60X signal name
18	HI_D1:2	SCAN_CTL†
17	HI_D1:1	SCAN_SIN†
16	HI_D1:0	SCAN_CLK†
15	HI_D0:7	SC_DRIVE†
14	HI_D0:6	CSE1†
13	HI_D0:5	CSE2†
12	HI_D0:4	CSE0†
11	HI_D0:3	BSCAN_EN*†
10	HI_D0:2	PCLK_EN*†
9	HI_D0:1	RESUME†
8	HI_D0:0	ESP_EN*†
7	HI_C1:7	RTC†
6	HI_C1:6	SYS_QUIESC*†
5	HI_C1:5	CKSTP_IN*†
4	HI_C1:4	QUIESC_REQ†
3	HI_C1:3	HP_SNP_REQ*†
2	HI_C1:2	SCAN_OUT†
1	HI_C1:1	RUN_NSTOP†
0	HI_C1:0	CKSTP_OUT*†

† **Signal not required for disassembly.**

Table 3–13 shows the probe section and channel assignments for the PPC603_4 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–13: 192-channel: PPC603_4 group channel assignments

Bit order	Section & probe	PowerPC 60X signal name
15	HI_C0:7	DBDIS*†
14	HI_C0:6	TLBISYNC*†
13	HI_C0:5	TBEN†
12	HI_C0:4	QACK*†
11	HI_C0:3	QREQ*†
10	HI_C0:2	CSE†

Table 3–13: 192-channel: PPC603_4 group channel assignments (cont.)

Bit order	Section & probe	PowerPC 60X signal name
9	HI_C0:1	CLK_OUT†
8	HI_C0:0	TCK†
7	LO_C1:7	TRST*†
6	LO_C1:6	TMS†
5	LO_C1:5	TDO†
4	LO_C1:4	TDI†
3	LO_C1:3	CKSTP_OUT*=†
2	LO_C1:2	CKSTP_IN*=†
1	LO_C1:1	MCP*†
0	LO_C1:0	SMI*†

† **Signal not required for disassembly.**

Table 3–14 shows the probe section and channel assignments for the PPC604 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–14: 192-channel: PPC604 group channel assignments

Bit order	Section & probe	PowerPC 60X signal name
7	LO_C0:7	TC2†
6	LO_C0:6	HALTED†
5	LO_C0:5	ARRAY_WR*†
4	LO_C0:4	RUN†
3	LO_C0:3	LSSD_MODE*†
2	LO_C0:2	L1_TSTCLK†
1	LO_C0:1	L2_TSTCLK†
0	LO_C0:0	not connected

† **Signal not required for disassembly.**

Table 3–15 shows the probe section and channel assignments for the clock probes (not part of any group), and the PowerPC 60X signal to which each channel connects.

Table 3–15: Clock channel assignments (not a group)

136-channel section & probe	192-channel section & probe	Clock or Qual	PowerPC 60X signal name	
CK:3	HI_CK:3, LO_CK:3	Clock (rising edge)	SYSCLK=	(SYSCLK)†
CK:2	HI_CK:2, LO_CK:2	Qual	DBB*=	(DBB*)
CK:1	HI_CK:1, LO_CK:1	Qual	TA*=	(TA*)
CK:0	HI_CK:0, LO_CK:0	Qual	TEA*=	(TEA*)

† **In an MPC601 or PPC601 SUT, connect the SYSCLK= signal to a 1X clock (such as the BCLK_EN* signal). Refer to *Requirements and Restrictions* in the *Getting Started* chapter for more detailed information on this clock.**

How Data is Acquired

This section explains how the module acquires PowerPC 60X signals using the TMS 540 probe adapter and application. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the PPC60X support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times when they are valid on the PowerPC 60X bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–2 shows one sample point and five master sample points.

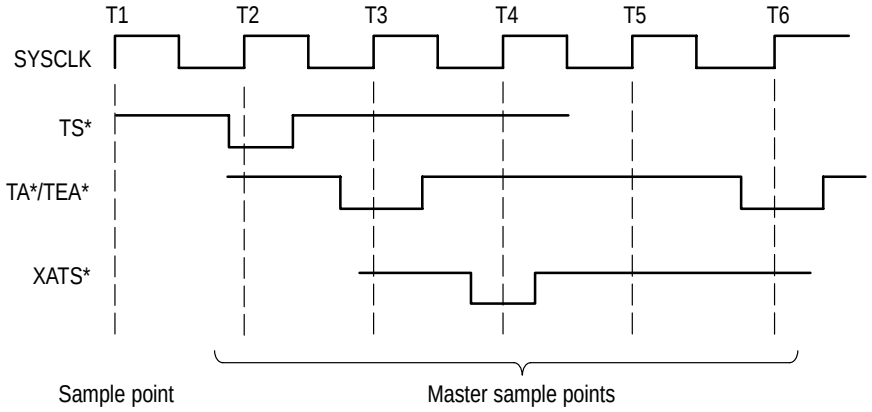


Figure 3–2: PowerPC 60X bus timing

T1 Clock Edge. The BG*, ABB*, and ARTRY* signals are logged in on this clock edge.

T2 Clock Edge. The A31-A0, TT3-TT1, TSIZ2-TSIZ0, XATS*, TBST*, TS*, TC0, SYSCLK, DBG*, DRTRY_ERLY*, DBWO*, and ARTRY_DATA* signals are logged in on this clock edge.

T3 Clock Edge. The DH31-DH0, DL31-DL0, TEA*, TA*, TT0, DBB*, AACK*, ARTRY*, DRTRY*, BR*, APE*, GBL*, BG*, ABB*, ARTRY_ERLY*, and XATS_B2* signals are logged in on this clock edge. Signals logged in on the T2 clock edge are also logged in except the A31-A0 signals.

T4 Clock Edge. The A31-A0, TT3-TT1, TSIZ2-TSIZ0, XATS*, TBST*, TS*, TC0, SYSCLK, DBG*, DRTRY_ERLY*, DBWO*, ARTRY_DATA*, BG*, ABB*, ARTRY_ERLY*, and XATS_B2 signals are logged in on this clock edge.

T5 Clock Edge. The A31-A0, TT3-TT1, TSIZ2-TSIZ0, XATS*, TBST*, TS*, TC0, SYSCLK, DBG*, DRTRY_ERLY*, DBWO*, and ARTRY_DATA* signals are logged in on this clock edge.

T6 Clock Edge. The DH31-DH0, DL31-DL0, TEA*, TA*, TT0, DBB*, AACK*, ARTRY*, DRTRY*, BR*, APE*, GBL*, BG*, ABB*, ARTRY_ERLY*, and XATS_B2* signals are logged in on this clock edge. Signals logged in on the T5 clock edge are also logged in except the A31-A0 signals.

Clocking Options

The clocking algorithm for the PowerPC 60X microprocessor support has two variations: DRTRY Cycles Included or DRTRY Cycles Excluded.

DRTRY Cycles. When DRTRY Cycles are included, the clocking stores the cycle right after the assertion of the TA* signal to check for the assertion of the DRTRY* signal. When DRTRY Cycles are excluded, the clocking will not store the cycle right after the assertion of the TA* signal to check for the assertion of the DRTRY* signal.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–4. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

The probe adapter does not provide access for the following MPC601 or PPC601 microprocessor signals:

- BLK_EN*
- 2X_PCLK
- BR*

The probe adapter also does not provide access to the Reserved pins (three) or to the Test pins (twenty).

The probe adapter does not provide access for the following MPC603 or PPC603 microprocessor signals:

- AVDD
- PLL_CFG0
- PLL_CFG1
- PLL_CFG2
- PLL_CFG3

Extra Channels

Table 3–16 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Channels not defined in a channel group by the TMS 540 software are logged in with the Master sample point.

Table 3–16: Extra module sections and channels

Module	Section: channels
136-channels	Qual:3-0
192-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

PPC60X Microprocessor Signal Names to PGA Socket Pin Numbers

You might want to connect to signals with other equipment, such as an oscilloscope, while analyzing activity in your SUT. You can connect to PPC60X microprocessor signals through the PGA socket on the probe adapter board since it does not have a microprocessor installed in it.

Table 3–17 shows PPC60X signal names and pin number connections between the PGA socket on the probe adapter and the various PPC60X microprocessors.

Table 3–17: PGA socket pin numbers to PPC60X signal names

PGA socket		Microprocessor pin number		
PPC60X signal	PGA pin no.	MPC601/PPC601	MPC603/PPC603	MPC604†
A0	G5	18	179	225
A1	G4	19	2	4
A2	H3	21	178	223
A3	H2	22	3	6
A4	H5	23	176	221
A5	J1	26	5	8
A6	J4	27	175	219
A7	J5	28	6	10
A8	J3	30	174	217
A9	K1	31	7	12
A10	K3	32	170	215
A11	K4	34	11	14
A12	L4	35	169	213

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
A13	L3	36	12	16
A14	M3	41	168	211
A15	M2	42	13	18
A16	M4	43	166	209
A17	M1	45	15	20
A18	N3	46	165	207
A19	N2	47	16	22
A20	N4	49	164	205
A21	N1	50	17	24
A22	P3	51	160	203
A23	P1	54	21	26
A24	P4	55	159	201
A25	P5	56	22	28
A26	Q5	58	158	199
A27	Q2	59	23	30
A28	Q4	60	151	191
A29	Q1	62	30	38
A30	R3	63	144	182
A31	R5	64	37	47
AACK*	E6	295	28	36
ABB*	E21	224	36	45
AP0	R1	67	231	295
AP1	S4	68	230	294
AP2	R2	69	227	292
AP3	S1	71	226	290
APE*	C17	231	218	276
ARRAY_WR*	C10	- - -	- - -	271
ARTRY*	F21	221	32	42
BG*	A5	298	27	35
BR*	A17	- - -	219	278
BSCAN_EN*	D5	299	- - -	- - -

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
CI*	F18	216	237	304
CKSTP_IN*	A13	258	- - -	- - -
CKSTP_IN*	D11	- - -	215	266
CKSTP_OUT*	D10	- - -	216	267
CKSTP_OUT*	S3	72	- - -	- - -
CLK_OUT	B10	- - -	221	280
CSE	B8	- - -	225	- - -
CSE0	G17	215	- - -	288
CSE1	G18	211	- - -	287
CSE2	G21	212	- - -	- - -
DBB*	F17	220	145	184
DBDIS*	L21	- - -	153	193
DBG*	E5	300	26	34
DBWO*	C5	297	25	32
DH0	U14	127	115	147
DH1	W13	126	114	145
DH2	T13	125	113	143
DH3	S13	123	110	142
DH4	U13	122	109	140
DH5	W12	121	108	138
DH6	S12	119	99	126
DH7	V12	118	98	124
DH8	U11	112	97	122
DH9	W10	111	94	121
DH10	T10	110	93	119
DH11	V10	108	92	117
DH12	U10	107	91	115
DH13	W9	106	90	114
DH14	T9	104	89	112
DH15	V9	103	87	110
DH16	T8	99	85	108

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
DH17	V8	98	84	107
DH18	U8	97	83	105
DH19	S8	95	82	103
DH20	W7	94	81	101
DH21	T7	93	80	100
DH22	V7	91	78	98
DH23	S7	90	76	96
DH24	U6	86	75	94
DH25	V6	85	74	93
DH26	T6	84	73	91
DH27	S6	83	72	89
DH28	W5	82	71	87
DH29	U5	81	68	86
DH30	V5	80	67	84
DH31	S5	75	66	82
DL0	L19	188	143	180
DL1	M17	185	141	178
DL2	N21	182	140	176
DL3	N18	181	139	174
DL4	N17	180	135	172
DL5	N19	178	134	170
DL6	P19	173	133	168
DL7	Q21	172	131	166
DL8	Q20	169	130	164
DL9	Q19	168	129	162
DL10	R21	167	126	160
DL11	R17	165	125	158
DL12	R20	161	124	156
DL13	R19	159	123	154
DL14	S21	157	119	152
DL15	S19	155	118	150

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
DL16	S17	151	117	148
DL17	T17	149	107	136
DL18	V17	148	106	135
DL19	U17	147	105	133
DL20	W17	145	102	131
DL21	T16	144	101	129
DL22	V16	143	100	128
DL23	S16	140	51	65
DL24	U16	139	52	67
DL25	V15	138	55	69
DL26	W15	136	56	71
DL27	T15	135	57	73
DL28	S15	134	58	75
DL29	U15	132	62	77
DL30	W14	131	63	79
DL31	T14	130	64	81
DP0	H19	203	38	49
DP1	J21	202	40	51
DP2	J18	201	41	53
DP3	J20	199	42	55
DP4	J19	198	46	57
DP5	K21	197	47	59
DP6	K17	195	48	61
DP7	K20	194	50	63
DPE*	E19	222	217	274
DRTRY*	B6	292	156	197
ESP_EN*	B9	275	- - -	- - -
GBL*	C16	233	1	2
HALTED	C12	- - -	- - -	269
HP_SNP_REQ*	B14	250	- - -	- - -
HRESET*	C8	279	214	265

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
INT*	D12	262	188	234
L1_TSTCLK	C7	- - -	204	255
L2_TSTCLK	E3	- - -	203	254
LSSD_MODE*	A7	- - -	205	256
MCP*	A15	- - -	186	232
PCLK_EN*	B7	285	- - -	- - -
QACK*	D7	- - -	235	- - -
QREQ*	L2	- - -	31	- - -
QUIESC_REQ	E12	256	- - -	- - -
RESUME	D9	277	- - -	- - -
RSRV*	C13	254	232	297
RTC	A10	273	- - -	- - -
RUN	D8	- - -	- - -	270
RUN_NSTOP	S2	74	- - -	- - -
SC_DRIVE	H17	210	- - -	- - -
SCAN_CLK	M21	187	- - -	- - -
SCAN_CTL	M20	184	- - -	- - -
SCAN_OUT	T5	78	- - -	- - -
SCAN_SIN	M18	186	- - -	- - -
SHD*	A17	235	- - -	- - -
SMI*	E18	- - -	187	233
SRESET*	C11	264	189	236
SYS_QUIESC*	B12	260	- - -	- - -
SYSCLK	E10	271	212	263
TA*	E13	290	155	195
TBEN	A6	- - -	234	299
TBST*	E16	236	192	241
TC0	E15	243	224	285
TC1	E14	251	223	283
TC2	C14	- - -	- - -	281
TCK	A11	- - -	201	252

Table 3–17: PGA socket pin numbers to PPC60X signal names (cont.)

PGA socket		Microprocessor pin number		
PPC60X signal	**PGA pin no.**	**MPC601/PPC601**	**MPC603/PPC603**	**MPC604†**
TDI	B13	- - -	199	250
TDO	D13	- - -	198	248
TEA*	E7	291	154	194
TLBISYNC*	C6	- - -	233	- - -
TMS	A12	- - -	200	251
TRST*	A9	- - -	202	253
TS*	H20	226	149	187
TSIZ0	B15	241	197	246
TSIZ1	B17	232	196	245
TSIZ2	B16	237	195	243
TT0	E17	228	191	239
TT1	E20	227	190	238
TT2	D14	248	185	231
TT3	D15	244	184	229
TT4	D16	238	180	227
WT*	F20	214	236	302
XATS*	D17	229	150	189

† **Pin information included for general purpose probing.**

Figure 3–3 shows the PGA socket on the probe adapter with the grid row and column labels for the pin numbers.

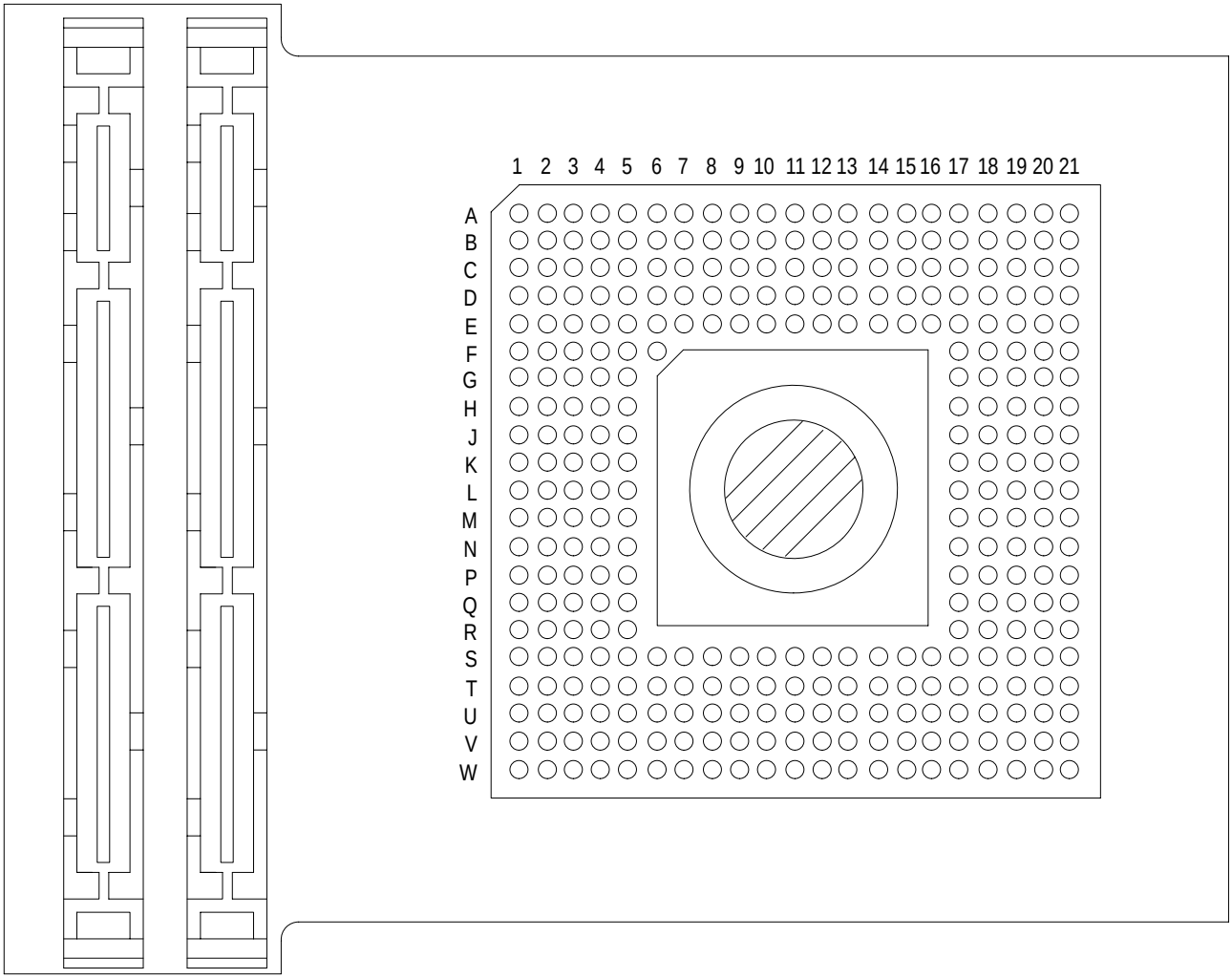


Figure 3–3: Grid row and column labels for the pin numbers on the PGA socket

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The probe adapter contains many 74FCT162244 devices that buffer all acquired signals. These devices have a chip-to-chip skew of 2 ns.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the PowerPC 60X probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

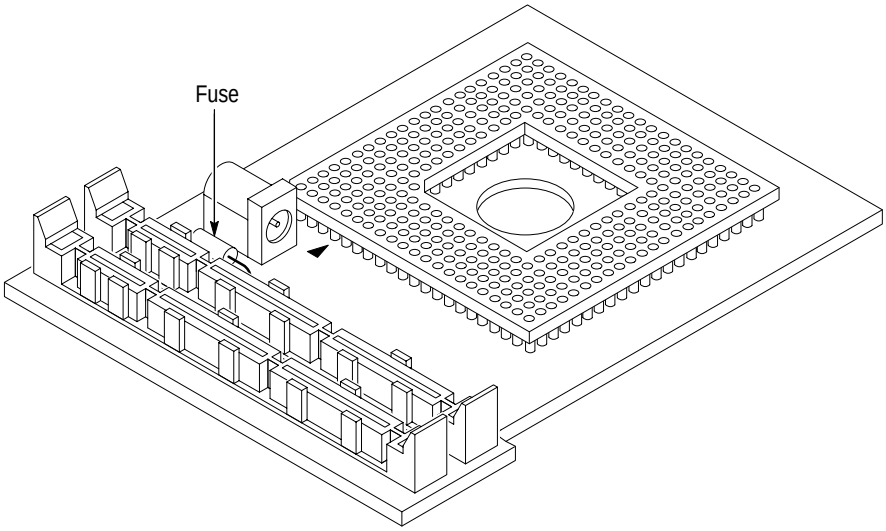


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 540 PowerPC 60X microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

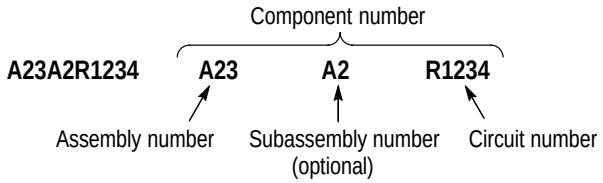
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
04222	AVX/KYOCERA DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
50434	HEWLETT–PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131–1008
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–3566–00			CKT BD ASSY:PGA–321 SOCKETED	80009	671356600
A1C120	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C130	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C140	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C150	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C200	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C210	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C250	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C350	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C400	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C450	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C530	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C540	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C550	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C630	290–5005–00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A1C655	290–5005–00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A1CR630	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31
A1J335	————————			SOCKET PGA:PCB,321 POS 21 X 21 SHORT PINS (SEE RMPL)		
A1F610	159–0059–00			FUSE,WIRE LEAD:5A,125V, (F610)	61857	SPI–5A
A1U120	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U130	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1U140	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U150	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U200	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U250	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U300	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U350	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U400	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U450	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U530	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U540	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439
A1U550	156–6982–00			IC,DIGITAL:FCTCMOS,BUFFER;16–BIT,RESISTOR TERMINATED OUTPUTS,3–STATE,SPECIALLY TESTED	61772	SCD5439

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 540 PowerPC 60X microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG MD 20879
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
14310	AULT INC	7300 BOONE AVENUE NORTH	MINNEAPOLIS MN 55428
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0588–00			1	PROBE ADAPTER:PPC60X,PGA–321,SOCKETED;TMS 540	80009	010058800
–1	174–3419–00			1	CA ASSY,SP:TLC,MICRO–STRIP;TLC,50 OHM,FEP,1.4NS, 13.0 L,100 POS,PLUG,LATCHING (W730)	00779	2–340014–5
–2	174–3418–00			1	CA ASSY,RF:TLC,MICRO–STRIP;TLC,50 OHM,FEP,PROP DELAY 1.4NS,12.0 L,100 POS,PLUG,LATCHING BOTH ENDS (W830)	00779	1–340014–0
–3	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER (P300)	26742	9618–302–50
–4	131–1857–00			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (J300)	58050	082–3644–SS10
–5	671–3566–00			1	CKT BD ASSY:PGA–321 SOCKETED,389–2071–00 WI RED	80009	671356600
–6	136–1283–00			2	SOCKET,PGA:PCB,321 POS,21 X 21,SHORT PINS (J335)	80009	136128300
–7	103–0369–01			1	MPC603 SUPPORT:MOT MPC603 ADAPTER,QFP–240 REQ. GENERIC PPC60X PROBE	80009	ORDER BY DESC
	103–0399–01			1	PPC603 SUPPORT:IBM PPC603 ADAPTER,QFP–240 REQ.GENERIC PPC60X PROBE	80009	ORDER BY DESC
–8	103–0398–00			1	MPC601 SUPPORT:MOT MPC601 ADAPER, QGP–304,REQ.GENERIC PPC60X PROBE	80009	ORDER BY DESC
–9	131–5947–00			2	CONN,BOX:PCB,MICRO–STRIP;FEMALE,STR,100 POS, 0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL, LATCHING,4 ROW,0.05 PCB,STAGGER (J730,J830)	00779	121289–7
–10	159–0059–00			1	FUSE,WIRE LEAD:5A,125V, (F610)	61857	SPI–5A
–11	131–5527–00			1	JACK,POWER DC:PCB,;MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,T IN,W/SWITCH,DC PWR JACK,2.0 MM (J510)	0LXM2	DJ005A
					STANDARD ACCESSORIES		
	070–9829–00			1	MANUAL,TECH:INSTRUCTION,PPC60X,DISSASEMBLER, TMS 540	80009	070–9829–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DE-SCRIPTION

Replaceable mechanical parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

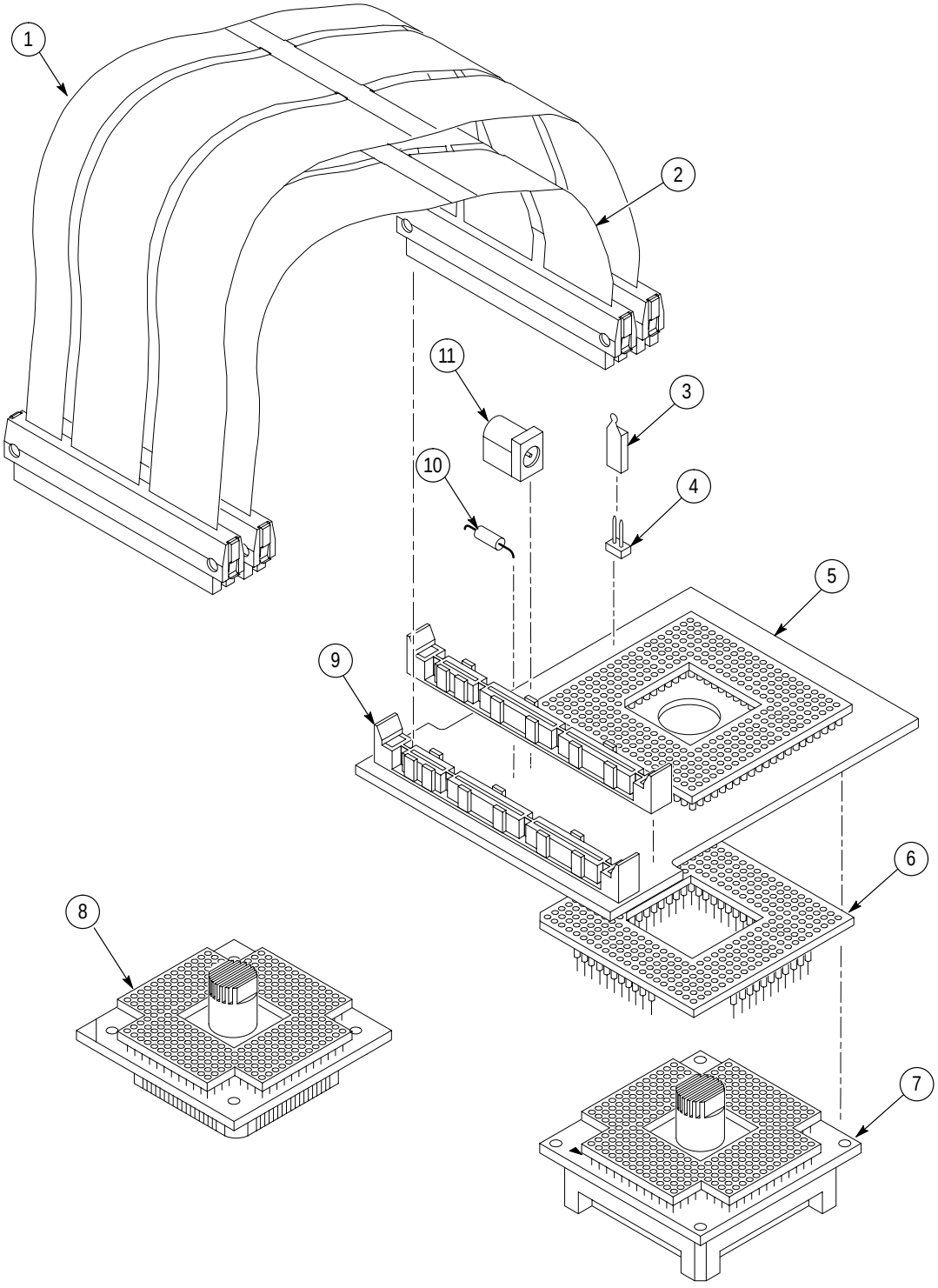


Figure 1: PowerPC 60X probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–0	010– 0582–00			1	ADAPTER,PROBE:192–CHANNEL,HIGH DENSITY PROBE	80009	010058200
–1	380–1095–00			1	HOUSING,HALF:UPPER,192 CHANNEL HIGH DENSITY PROBE	80009	380109500
–2	211–0152–00			4	SCR,ASSEM WSHR:4–40 X 0.625,PNH,BRS,NP,POZ	TK0435	ORDER BY DESC
–3	131–5947–00			2	CONN BOX:CPCB, MICRO–STRIP;FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.124 TAIL, LATCHING, 4 ROW, 0.05 PCB, STAGGER (J150, J250)	80009	131594700
–4	671–3395–00			1	CKT BD ASSY:192–CHANNELS,HIGH DENSITY PROBE	80009	671339500
–5	380–1096–00			1	HOUSING,HALF:LOWER,192 CHANNEL HIGH DENSITY PROBE	80009	380109600
–6	348–0070–01			2	PAD,CUSHIONING:2.03 X 0.69 X 0.18 SI RBR	85471	ORDER BY DESC
–7	131–4917–00			8	CONN,HDR CPCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLF X 0.110 TAIL,20 BOLD, TUBE, HIGH TEMP (J300,J340J400,J440,J500,J640,J600)	53387	131491700
–8	131–5267–00			5	CONN,HDR CPCB,;MALE,STR,2 X 40.O.1 CTR,0.234 MLG X 0.110 TAIL, 30 GOLD (J310,J320,J330,J340,J350,J360,J370,J410,J420,J430,J450,J460,J470,J510,J520,J530,J550,J560,J570,J610,J620,J630,J650,J660,J670)	53387	131526700

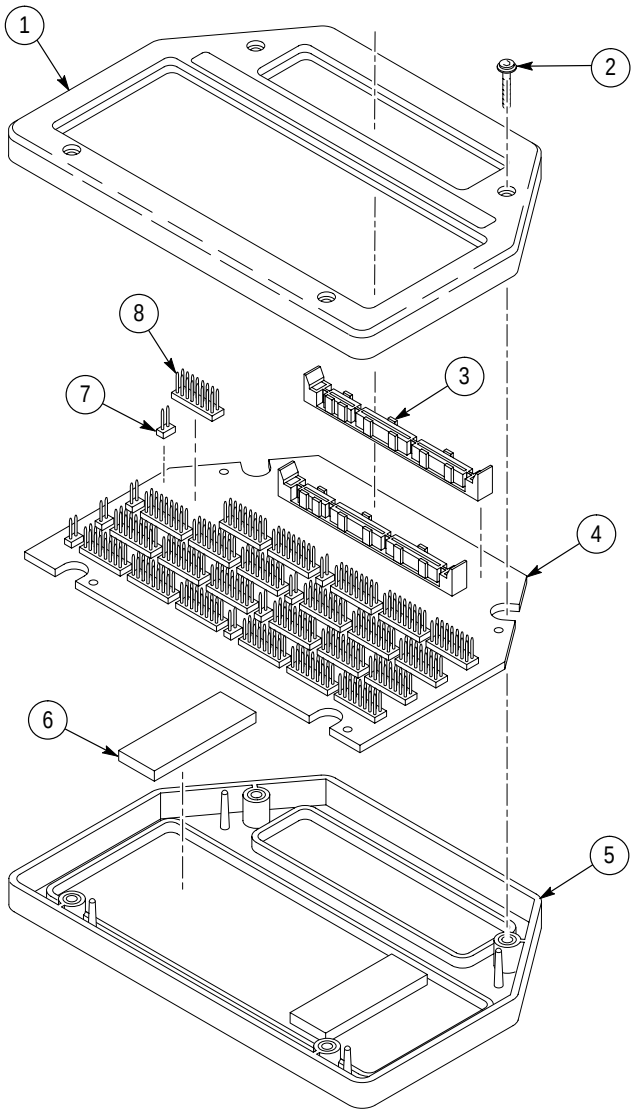


Figure 2: 192-Channel High-Density Probe exploded view

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